NC2008 Multi Output Clock Generator IC

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Overview

The NC2008 is a highly integrated multi output clock generator and signal translation device. This design implementation is extremely flexible in providing low noise frequency generation and/or signal level translation capability. The design architecture incorporates Connor-Winfield's second generation analog PLL technology to provide up to 17 output(s) at frequencies ranging from 1Hz to 800 MHz, depending upon the input reference option chosen. One or two external signal sources determine the output characteristics for phase noise and jitter performance for any combination of eight differential or 17 single ended clock outputs with output jitter performance options of sub 100fs RMS (12 kHz to 20MHz).

Configurations can be controlled using I2C interface, external EE PROM or can be pre configured in nonvolatile memory (OTP) at the factory. One or two external signal sources can be accepted from a crystal unit, a single ended LVCMOS signal, a differential (LVDS or LVPECL) signal or a combination of those. When using a crystal unit, 100fs jitter performance is achievable.

Typical Applications

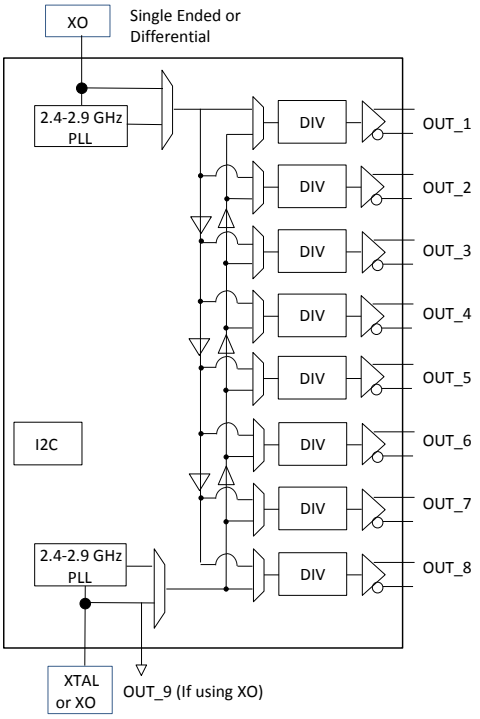
- Clock Generation
- Multi output clock buffer
- Signal level translation

Features

- 1Hz to 800 MHz clock output frequency range
- Eight differential or up to 17 single ended Low Jitter Clock Outputs
- Programmable output transmitters (programmable as either 1 LVPECL, 1 LVDS or 2x LVCMOS output)
- 20 bit divider capability at output transmitters 1-8.
- Low jitter clock outputs of less than .25ps RMS (12kHz to 20MHz) with options for sub 100fs.
- Signal translation from LVCMOS to LVPECL/LVDS or Vice versa
- External EEProm for loading or I2C Interface for system communication
- 3.3V supply
- 8x8 mm 68 pin QFN surface mount package

NC2008 Functional Block Diagram

NC2008
Block Diagram



RoHS COMPLIANT

Bulletin	TM134
Revision	03
Date	05 Jan 2021

Specifications

Parameter	Specification
Voltage	3.3V +/- 5%
Power	Based on configuration (100ma with outputs tri-stated) Outputs add: LVPECL 50ma, LVDS 20Ma, LVCMOS 8 ma
Temperature	-40 to 85 C Industrial temp range operation
Reference Frequency for PLL	Crystal unit (40-160MHz), differential (LVDS or LVPECL) signal up to 800MHz or Single ended clock input 40MHz- 125MHz
Low Jitter Clock Output Frequency	1 Hz to 800 MHz
Output Transmitter	Programmable to be either LVPECL, LVDS or 2x LVCMOS
Divider Capability	20 bit
Dimensions	8 x 8x 1mm 68 pin QFN package

NC2008 General Description

The NC2008 is a highly integrated PLL clock generator ASIC. The design architecture incorporates a sophisticated analog PLL scheme to provide up to 17 low jitter clock outputs at frequencies from 1.5 kHz to 800 MHz from either one or two independent analog integer PLLs. These outputs can be generated from one or two reference input signals at frequencies from 5 MHz to 800 MHz. The reference input signal source can be supported by a crystal, an external single ended LVCMOS clock source, a differential clock source (LVPECL/LVDS) or a combination of these options. The design incorporates two analog PLLs and eight output transmitter circuits, each with 20 bit divider capability. The two PLLs can be used in tandem to share the eight output circuits or all eight can be accessed by one or the other exclusively. Clocks can be generated using the on board oscillator and passed through directly to the output transmitter ports or the input signal can be routed through an APLL with an integrated VCO in the range of 2.4GHz to 2.95 GHz. An internal pre divider makes the usable VCO range of 1.2GHz to 1.475 GHz to be further divided at each individual output transmitter port.

NC2008 Analog PLL Chain Description

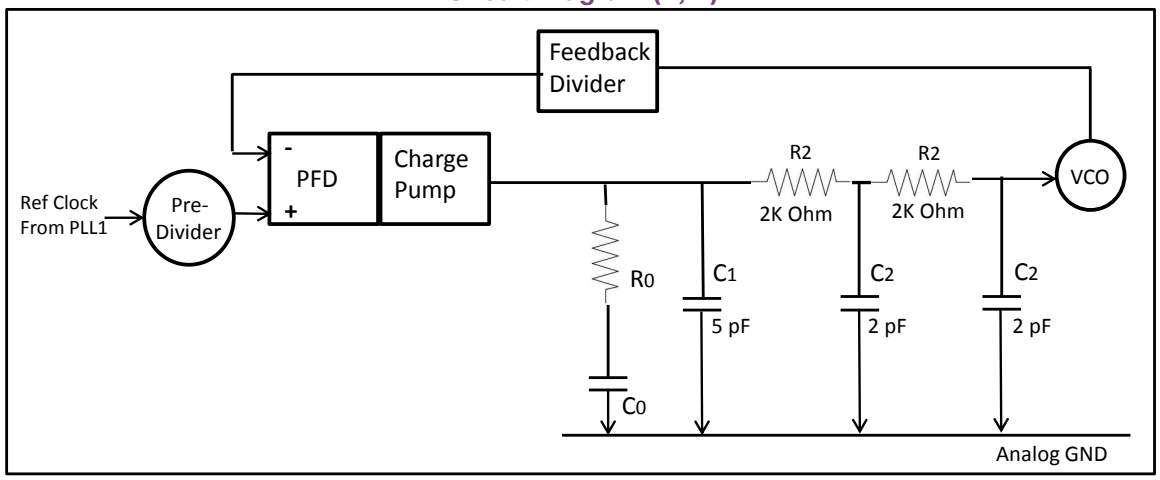
The NC2008 is designed to support two simultaneous, independent frequency domains which share four banks of two clock output stages each. The NC2008 consists of two (2) independent analog PLL stages, referred to as XPLL and YPLL. In each X and Y side, the PLL stage can accept an incoming signal and lock to an internal VCO in the usable range of 1.2GHz to 1.475 GHz. Each of eight output transmitters can be divided by any integer value with up to 20 bit resolution (1048576) to generate clock outputs divided from the VCO frequency chosen. The eight independent programmable clock output transmitter circuits have 3-in-1 programmable output logic capability. Each transmitter circuit can be configured as either 2x LVCMOS outputs, 1 LVDS output or 1 LVPECL output. Depending upon the external XTAL/XO configuration used, clock outputs can be generated in a frequency range from 1Hz to 800MHz (limited to 180MHz for LVCMOS outputs) and can provide output jitter performance of less than 100fs RMS over the integration range of 12 kHz to 20MHz. The two X and Y PLL stages can be used in tandem to share the output stages or independently with all outputs driven from an input from only one side of the chip. There is a fixed skew delay through the output banks of the chip as described below in the Output Transmitter Ports section.

X-Side PLL Chain Description

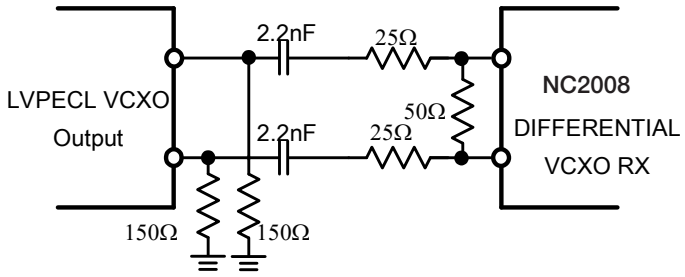
On the X side of the chip, XPLL can accept a reference signal input from a single ended LVCMOS signal or differential XO or clock signal at frequencies from 1MHz to 800MHz. For best jitter performance, an XO frequency of 40MHz or higher should be used as an input to the XPLL unless the signal is being passed through to the output transmitters directly. The input frequency enters the chip into a MUX that allows for the signal to be passed directly through to the output transmitters/divider ports or be sent as an input to the XPLL to synthesize output frequencies from the internal VCO divided at the output transmitter ports. Outputs derived from XPLL, depending upon frequency, will generally provide jitter performance levels of < 250fs over the integrated band of 12 kHz to 20 MHz.

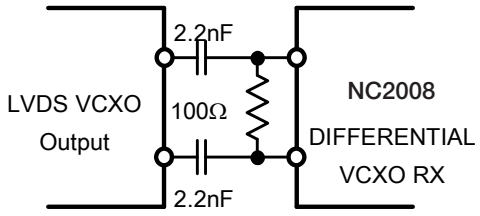
ADDR	NAME	TYPE	BITS	DEFAULT	DESCRIPTION
0x04	XPLL Mode	RW	2 - 0	0	XPLL Mode 0, 3: power down 1: single-end clk 2: differential clk

PLL Circuit Diagram (X, Y)



Differential XO termination recommendation in to pins XRX_P and XRX_N





XPLL BYPASS Mode

The input XO or signal to X side can be passed directly through to the output transmitters/divider ports To bypass the XPLL and send the reference input source to the divider/transmitter ports directly, the XPLL Output Source register setting should be set as "Bypass". A clock signal into the X side reference input will then be passed directly to the output transmitters chosen. Outputs sent to the output ports in bypass mode general retain their jitter character adding minimal jitter.

ADDR	NAME	TYPE	BITS	DEFAULT	DESCRIPTION
0x39	XPLL Output Source	RW	0	1	XPLL output source 0: Bypass 1: XPLL

Y-Side PLL Chain Description

On the Y side of the chip, YPLL can be supported by a crystal unit from 10MHz to 170MHz (fundamental mode only) or single ended clock signal at frequencies from 1MHz to 180MHz. For best jitter performance, a crystal or an LVCMOS clock frequency of 40MHz or higher should be used as an input to the YPLL unless the signal is being passed through to the output transmitters directly. An additional output (Output 9) is available when using a single ended XO on the Y side PLL. The XO nominal frequency will bypass directly to Output 9, but with inverted phase, from the input XO (as well as the outputs generated in the transmitter ports when used).

Outputs derived from YPLL, depending upon frequency, will generally support jitter performance levels of < 250fs over the integrated band of 12 kHz to 20 MHz.

ADDR	NAME	TYPE	BITS	DEFAULT	DESCRIPTION
0x05	YPLL Mode	RW	0	0	YPLL Mode 0: power down 1: power up

YPLL BYPASS Mode

The crystal input or the XO/ LVCMOS signal to Y side can be passed directly through to the output transmitters/divider ports To bypass the YPLL and send the reference input source to the divider/transmitter ports directly, the YPLL Output Source register setting should be set as "Bypass". A clock signal into the Y side reference input will then be passed directly to the output transmitters chosen. Outputs sent to the output ports in bypass mode general retain their jitter character adding minimal jitter.

ADDR	NAME	TYPE	BITS	DEFAULT	DESCRIPTION
0x3a	YPLL Output Source	RW	0	1	YPLL output source 0: Bypass 1: YPLL

Eight 3-in-1 Programmable Output Transmitter

Output transmitter ports 1 through output 8 consist of programmable 3-in-1 transmitters that can be configured to output either (2) LVCMOS or 1 LVDS or 1 LVPECL logic signal. Output transmitters can be powered down if not in use. When using LVCMOS mode, outputs can be generated on both output pins (P and N) of the output transmitter, or, one or the other. Polarity of the LVCMOS output at each pin is controllable.

ADDR	NAME	TYPE	BITS	DEFAULT	DESCRIPTION
0x31	Output1 Transmitter Mode	RW	4 - 0		Output1 transmitter mode, Bit[2:0] 0, 6, 7: power down, 1: LVDS 2: LVPECL 3: LVCMOS, P on, N off 4: LVCMOS, P off, N on 5: LVCMOS, P on, N on When transmitter is in LVCMOS mode, Bit[5:4] control polarity of output Bit4 0: P is not inverse, 1: P inverse Bit5 0: N is not inverse, 1: N is inverse

Output Transmitter Port Description

Output transmitter ports 1 through 8 are divided into four output “banks”. Each of the four output banks must be controlled as a unit. Bank0 (Output transmitters 1 and 2), Bank1 (Output transmitters 3 and 4), Bank2 (Output transmitters 5 and 6), and Bank3 (Output transmitters 7 and 8) represent four “banks” of outputs that can be controlled independently from each X and Y side of the chip. Either the X side or the Y side of the chip can access all four output banks, thus eliminating the requirement to use both sides X and Y in all applications. However, X and Y side clock signals must access output banks in order and must stop at the first output bank placed in use by the alternate side. For example, if X side uses banks 0, 1 and 2, Y side can only access bank 3 (outputs transmitters 7 and 8) or if Y side uses banks 3 and 2 (output transmitters 8,7 and 6,5), X side can only access bank 1 and 0 (outputs transmitters 1,2 and 3,4).

ADDR	NAME	TYPE	BITS	DEFAULT	DESCRIPTION
0x3b	Output Source Selection	RW	2 - 0	0	Output 1 ~ 8 source selection, output can come from either xpll or ypll, the arrangement are as follows, 0,5,6,7: xpll -> 1,2,3,4,5,6,7,8 1: xpll -> 1,2,3,4,5,6 ypll ->7,8 2: xpll -> 1,2,3,4 ypll -> 5,6,7,8 3:xpll -> 1,2 ypll -> 3,4,5,6,7,8 4:ypll -> 1,2,3,4,5,6,7,8

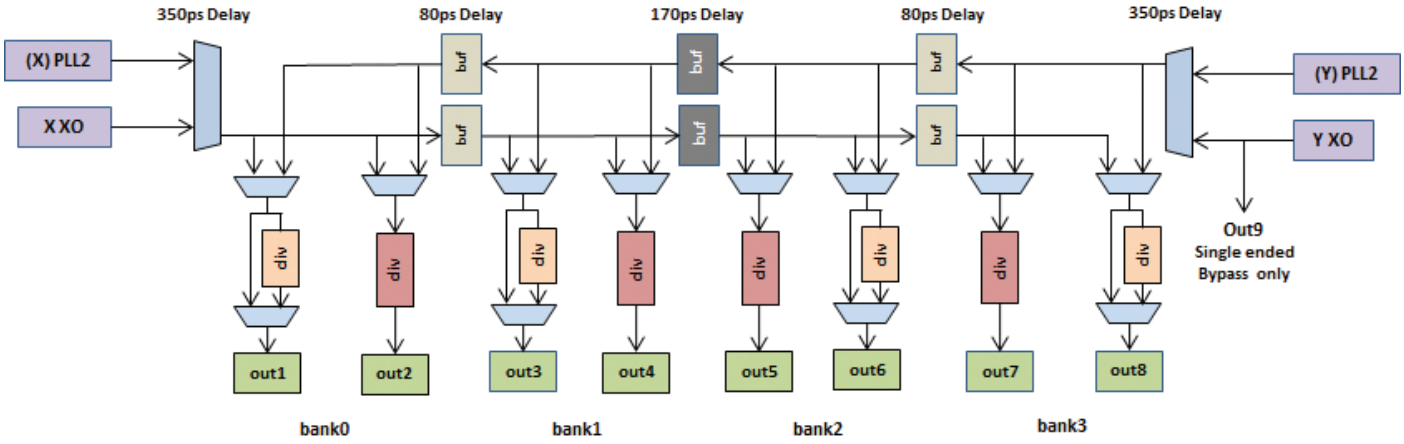


Diagram 1 Detailed Output Port Diagram
(when using an LVCMOS XO on Y side PLL)

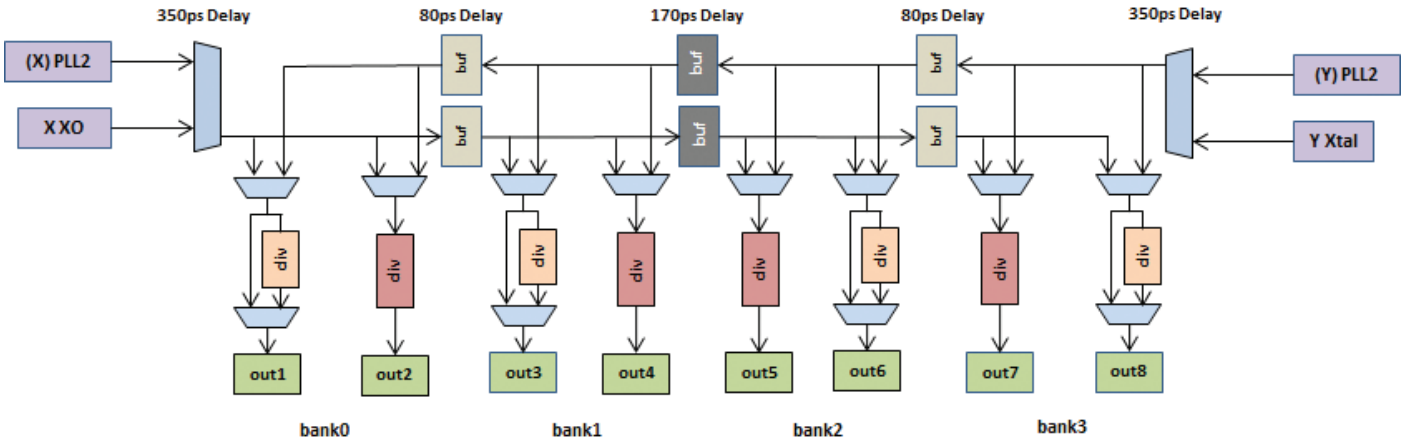


Diagram 2 Detailed Output Port Diagram
(when using a Crystal Unit on Y side PLL)

Output Skew Description

The skew between clock outputs is constant but will exhibit a cumulative delay relative to each other based on the clock signal traveling through MUXs and Buffers. This will be dependent upon how the output banks are configured from each X and Y side. Delay time are identified in Diagram 1 and 2.

Output 9

On the Y side, output 9 has been provided for use when a single ended clock signal is used as the reference input to the Y side PLL or in bypass mode. Output 9 acts as a low jitter buffer that directly bypasses the respective XO signal in and out of the NC2008 resulting in the least amount of additive jitter (about 10fs). This output is intended to be used for ultra-low jitter performance requirements when attempting to retain the characteristics of a low jitter source. If a crystal unit is used as reference source on the Y side PLL, Output 9 is not available since that pin is used as one pole of the crystal unit input. (see Diagram 2)

20 bit Divider Circuits

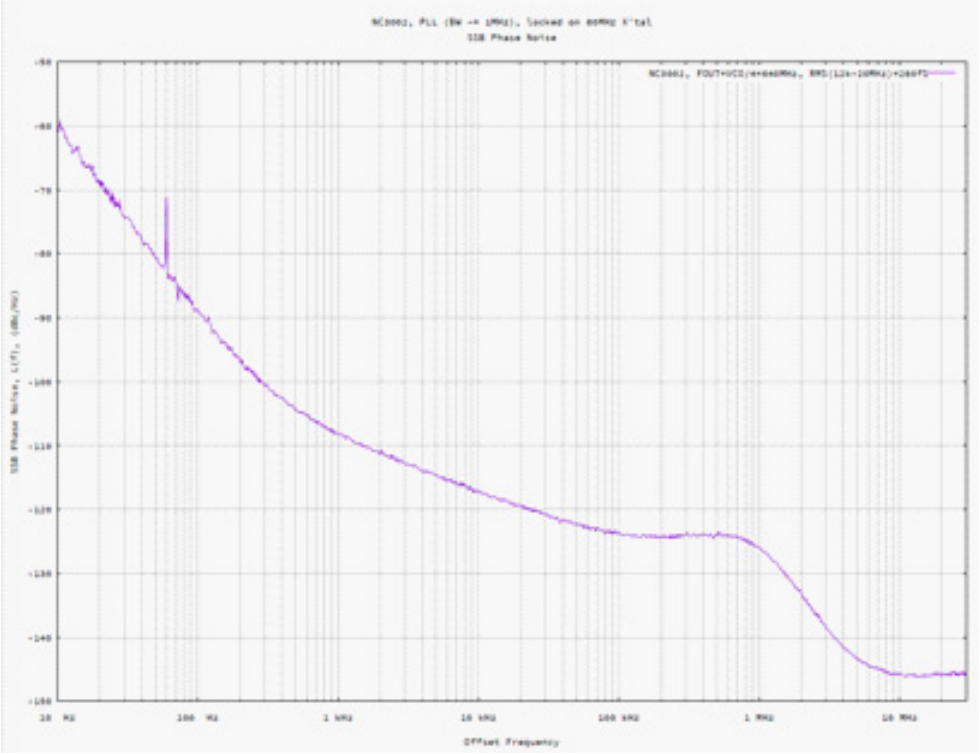
Output ports 1-8 have 20 bit divider capability (any integer value from 1-1,048,576). Regardless if the frequency is generated by the VCO or if it is bypassed through from the reference input source, the divider circuit can be used to generate divided frequencies. For instance, using a 1MHz input clock source in bypass mode, can achieve a 1Hz output through the divider circuit. Please note, low frequency input options are only available in bypass mode as inputs to the X and Y PLL requires a minimum of 40 MHz input frequency.

ADDR	NAME	TYPE	BITS	DEFAULT	DESCRIPTION
0x40 ~ 0x42	Output 1 Divider Value	RW	19 - 0	0	20 bit OUTPUT1 divider value

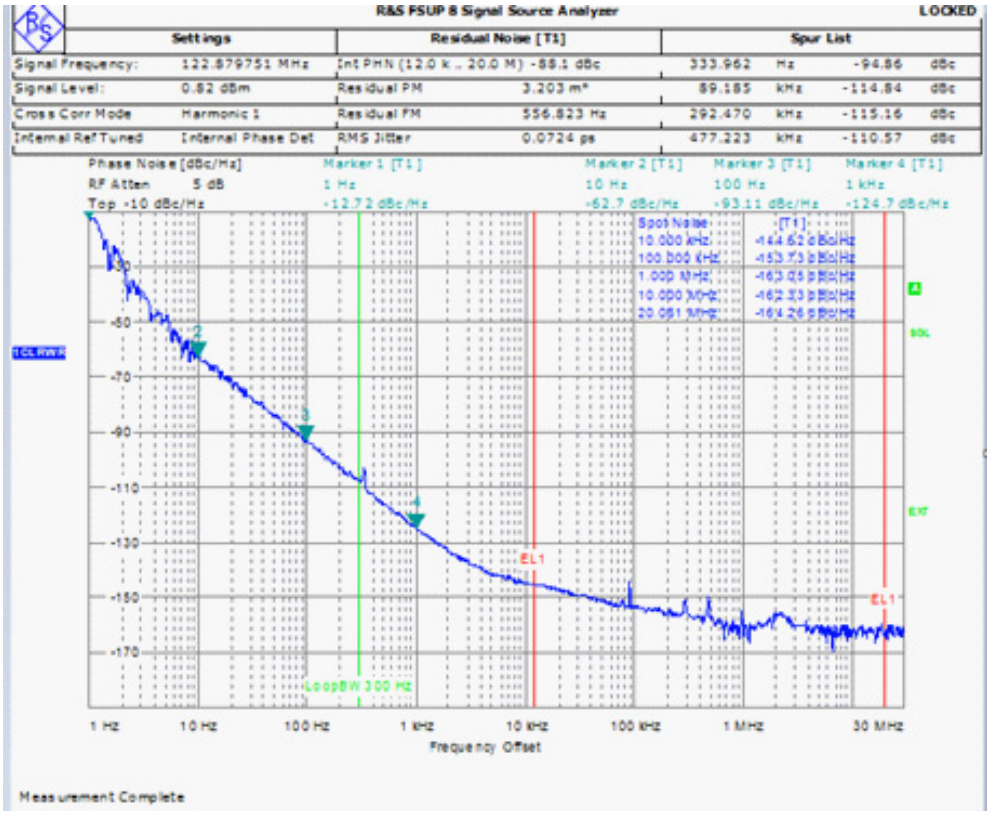
Symmetry Control for low value odd dividers

Output transmitter circuits #2, 4, 5 and 7 have, by default, output symmetry control when dividing by a single digit odd integer value. In circumstances which require dividing the VCO output frequency by values of 3, 5, 7 or 9, one of these output transmitter circuits should be used to achieve 50/50 duty cycle. When using an odd divider value of greater than nine (9), symmetry control is generally not required to maintain reasonable symmetry in the output. The output ports offering symmetry control do not allow for a direct by-pass through of the reference input frequency and require dividing at the output transmitter circuit by a minimum by 2. Output ports 1, 3, 6 and 8 can by-pass the divider circuit entirely or can divide by any integer number up to the 20bit value.

Output Phase Noise Characteristics Examples

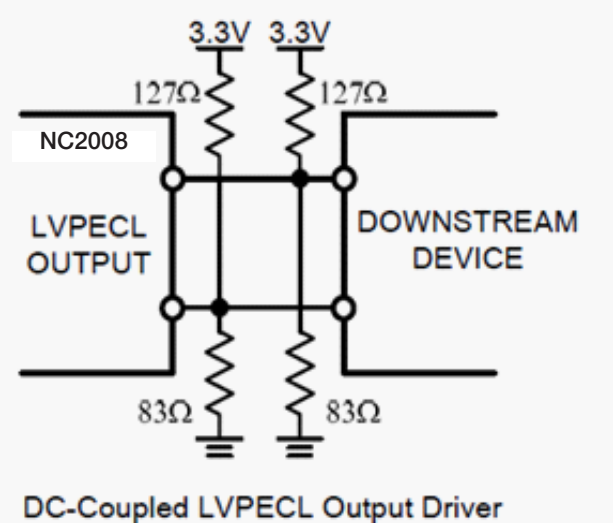


Phase noise generated from PLL2: 640MHz using 80MHz XO
260fs (12kHz-20MHz)

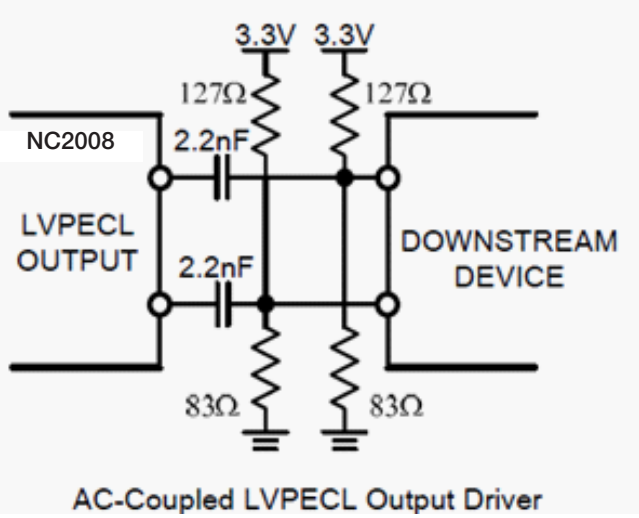


Phase noise generated from 156.25MHz Crystals 93fs (q2kHz-20MHz)

LVPECL Suggested Termination



DC-Coupled LVPECL Output Driver



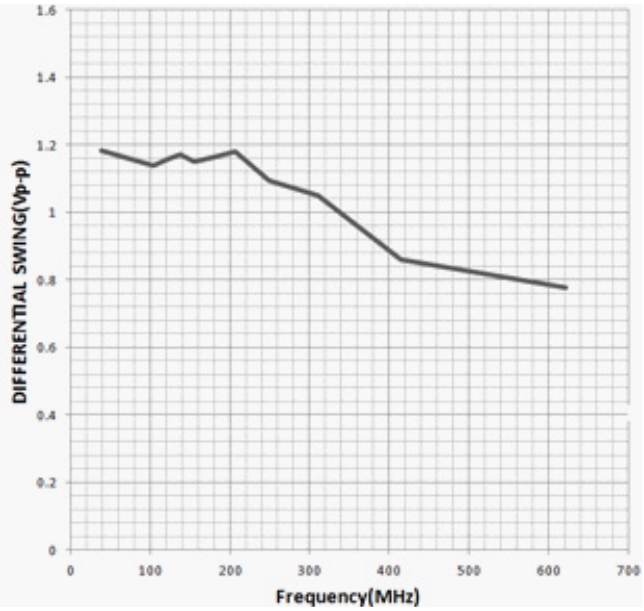
AC-Coupled LVPECL Output Driver

LVPECL Current Consumption

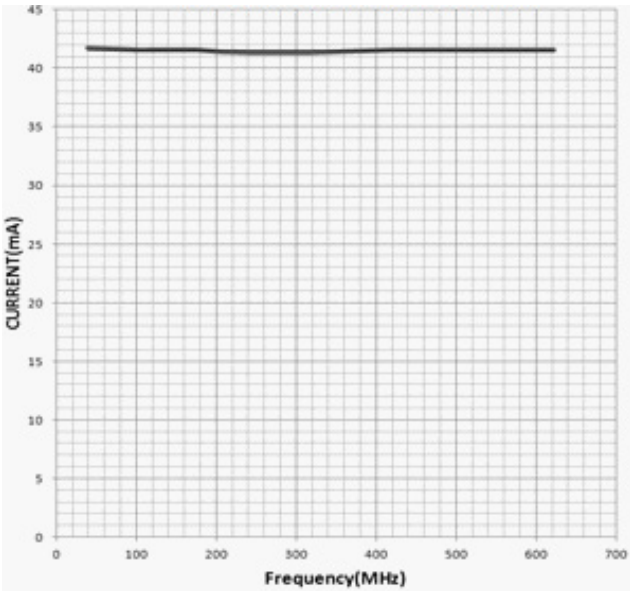
fvco=1.244GHz, fvcxo=38.88MHz,ftcxo=20MHz

OUTPUT FREQUENCY (MHz)	DUTY CYCLE (%)	RISE TIME (20%~80%)(ps)	CURRENT CONSUMPTION (mA)	DIFFERENTIAL SWING (Vp-p)
38.88	50.09	590	41.69	1.183
103.681	49.97	570	41.59	1.139
113.108	45.44	560	41.59	1.148
124.417	49.98	570	41.57	1.161
138.239	44.49	520	41.53	1.171
155.519	49.98	530	41.56	1.152
177.74	43.06	570	41.56	1.163
207.362	50.1	510	41.41	1.182
248.836	42	430	41.34	1.095
311.054	50.14	500	41.32	1.049
414.736	35.64	370	41.53	0.86
622.115	51.05	270	41.56	0.778

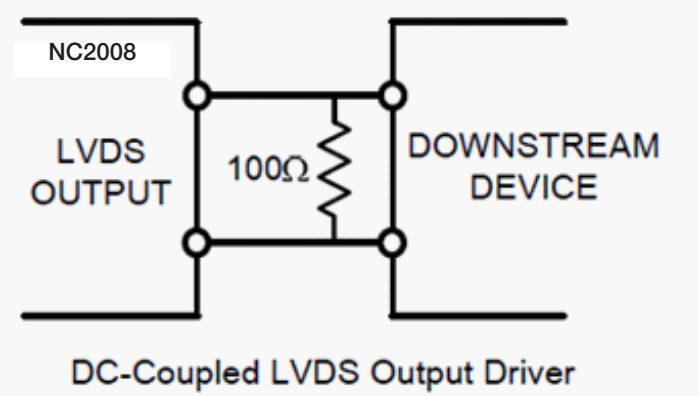
LVPECL Differential Swing



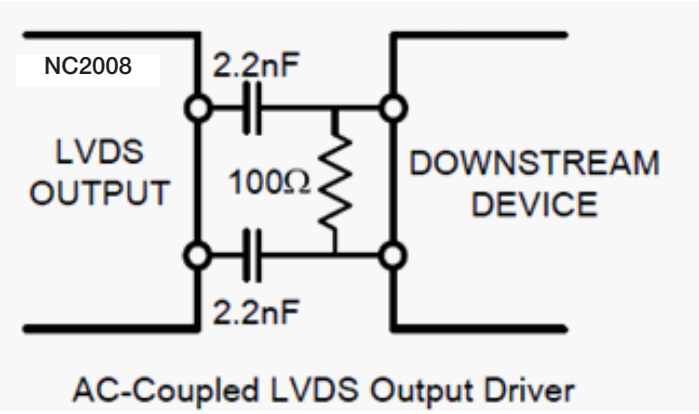
LVPECL Current Consumption



LVDS Suggested Termination



DC-Coupled LVDS Output Driver



AC-Coupled LVDS Output Driver

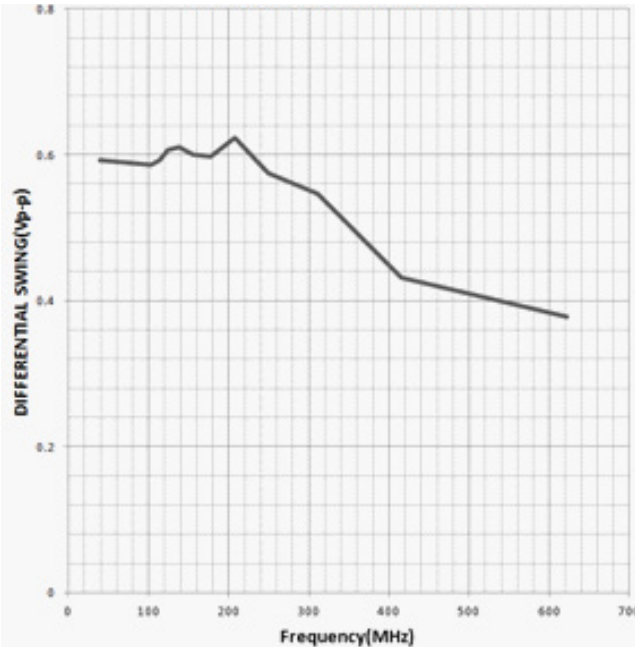
LVDS Current Consumption

fvco=1.244GHz, fvcxo=38.88MHz,ftcxo=20MHz

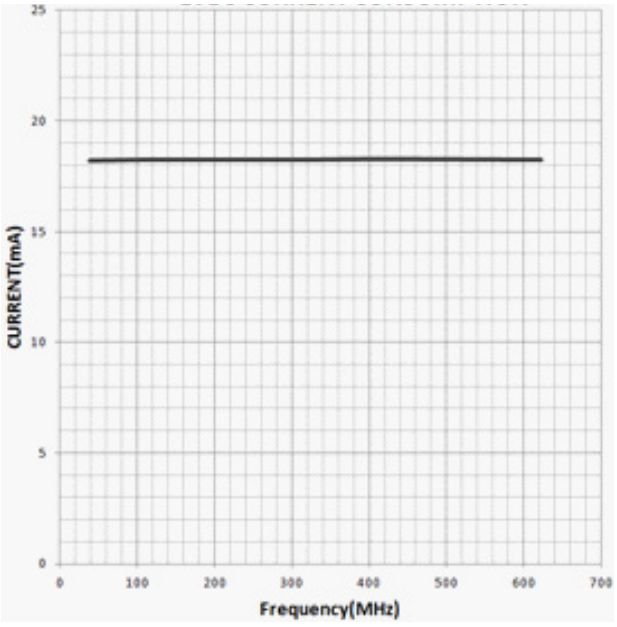
OUTPUT FREQUENCY (MHz)	DUTY CYCLE (%)	RISE TIME (20%~80%)(ps)	CURRENT CONSUMPTION (mA)	DIFFERENTIAL SWING (Vp-p)
38.8815	49.97	700	18.18	0.593
103.68	50.18	620	18.26	0.586
113.107	50.46	600	18.26	0.593
124.414	50.21	610	18.26	0.606
138.241	50.52	580	18.26	0.61
155.52	50.26	600	18.26	0.6
177.737	50.81	610	18.26	0.598
207.363	50.52	600	18.25	0.623
248.832	50.8	450	18.25	0.575
311.05	50.62	580	18.26	0.547
414.733	49.57	250	18.27	0.431
622.108	50.9	220	18.24	0.378

LVDS Output Common-Mode Voltage = 1.27V

LVDS Differential Swing



LVDS Current Consumption



NC2008 Register Table

ADDR	NAME	TYPE	BITS	DEFAULT	DESCRIPTION
0x00 ~ 0x01	Chip ID	RO	15 - 0	0x2008	Chip ID, it reflects the current product ID,
0x02	Chip Revision	RO	7 - 0	2	Chip Revision
0x03	Chip Sub-Revision	RO	7 - 0	1	Chip Sub revision
0x04	XPLL Mode	RW	2 - 0	0	XPLL Mode 0, 3: power down 1: single-end clk 2: differential clk
0x05	YPLL Mode	RW	0	0	YPLL Mode 0: power down 1: power up
0x10	XPLL Pre Divider Value	RW	2 - 0	0	XPLL pre divider value
0x11	XPLL FB Divider Value	RW	6 - 0	0	XPLL feedback divider value
0x12	XPLL KVCO	RW	0	0	XPLL kvco 0: small 1: large
0x13	XPLL C0 Value	RW	0	0	XPLL C0 value 0: 100 pF 1: 200 pF
0x14	XPLL R0 Value	RW	3 - 0	0	XPLL R0 Value 0: 3k, 1: 4.2k, 2: 6k, 3: 8.4k, 4:12k, 5: 16.8k, 6: 12k, 7: 16.8k 8: 24k, 9: 33.6k, 10: 24k, 11: 33.6k , 12: 46.3k, 13: 66k, 14: 46.3k, 15: 66k
0x15 ~ 0x16	XPLL Charge Pump Current	RW	10 - 0	100	XPLL charge pump current value, 1.25uA x reg_value
0x20	YPLL2 Pre Divider Value	RW	2 - 0	0	YPLL2 pre divider value
0x21	YPLL2 FB Divider Value	RW	6 - 0	0	YPLL2 feedback divider value
0x22	YPLL2 KVCO	RW	0	0	YPLL2 kvco 0: small 1: large
0x23	YPLL2 C0 Value	RW	0	0	YPLL2 C0 value 0: 100 pF 1: 200 pF
0x24	YPLL2 R0 Value	RW	3 - 0	0	YPLL2 R0 Value 0: 3k, 1: 4.2k, 2: 6k, 3: 8.4k, 4:12k, 5: 16.8k, 6: 12k, 7: 16.8k 8: 24k, 9: 33.6k, 10: 24k, 11: 33.6k , 12: 46.3k, 13: 66k, 14: 46.3k, 15: 66k
0x25 ~ 0x26	YPLL2 Charge Pump Current	RW	10 - 0	100	YPLL2 charge pump current value, 1.25uA x reg_value
0x31	Output1 Transmitter Mode	RW	4 - 0		Output1 transmitter mode, Bit[2:0] 0, 6, 7: power down, 1: LVDS 2: LVPECL 3: LVCMOS, P on, N off 4: LVCMOS, P off, N on 5: LVCMOS, P on, N on When transmitter in LVCMOS mode, Bit[5:4] control polarity of output Bit4 0: P is not inverse, 1: P inverse Bit5 0: N is not inverse, 1: N is inverse

NC2008 Register Table continued

ADDR	NAME	TYPE	BITS	DEFAULT	DESCRIPTION
0x32	Output2 Transmitter Mode	RW	4 - 0	0	Same as Output1 Transmitter Mode
0x33	Output3 Transmitter Mode	RW	4 - 0	0	Same as Output1 Transmitter Mode
0x34	Output4 Transmitter Mode	RW	4 - 0	0	Same as Output1 Transmitter Mode
0x35	Output5 Transmitter Mode	RW	4 - 0	0	Same as Output1
0x36	Output6 Transmitter Mode	RW	4 - 0	0	Same as Output1 Transmitter Mode
0x37	Output7 Transmitter Mode	RW	4 - 0	0	Same as Output1 Transmitter Mode
0x38	Output8 Transmitter Mode	RW	4 - 0	0	Same as Output1 Transmitter Mode
0x39	XPLL Output Source	RW	0	1	XPLL output source 0: Bypass 1: XPLL
0x3a	YPLL Output Source	RW	0	1	YPLL output source 0: Bypass 1: YPLL
0x3b	Output Source Selection	RW	2 - 0	0	Output 1 ~ 8 source selection, output can come from either xpll or ypll, the arrangement are as follows, 0,5,6,7: xpll -> 1,2,3,4,5,6,7,8 1: xpll -> 1,2,3,4,5,6 ypll ->7,8 2: xpll -> 1,2,3,4 ypll -> 5,6,7,8 3:xpll -> 1,2 ypll -> 3,4,5,6,7,8 4: ypll -> 1,2,3,4,5,6,7,8
0x40 ~ 0x42	Output 1 Divider Value	RW	19 - 0	0	20 bit OUTPUT1 divider value
0x43 ~ 0x45	Output2 Divider Value		RW	19 - 0	020 bit OUTPUT2 divider value
0x46 ~ 0x48	Output3 Divider Value	RW	19 - 0	0	20 bit OUTPUT3 divider value
0x49 ~ 0x4b	Output4 Divider Value	RW	19 - 0	0	20 bit OUTPUT4 divider value
0x4c ~ 0x4e	Output5 Divider Value	RW	19 - 0	0	20 bit OUTPUT5 divider value
0x4f ~ 0x51	Output6 Divider Value	RW	19 - 0	0	20 bit OUTPUT6 divider value
0x52 ~ 0x54	Output7 Divider Value	RW	19 - 0	0	20 bit OUTPUT7 divider value
0x55 ~ 0x57	Output8 Divider Value	RW	19 - 0	0	20 bit OUTPUT8 divider value

Package Outline

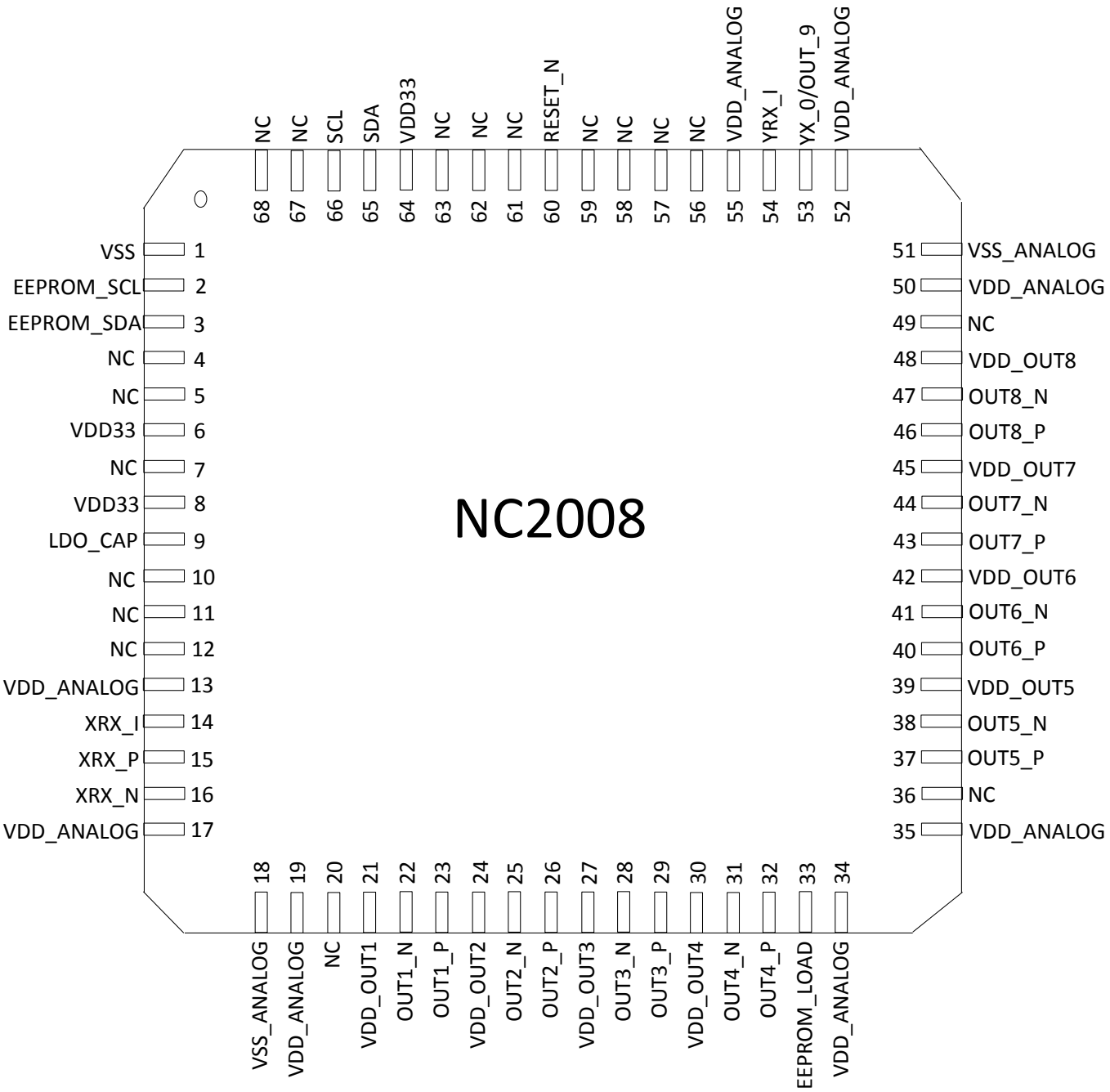


Diagram 3: Pin Out Map

NC2008 Pin Assignments

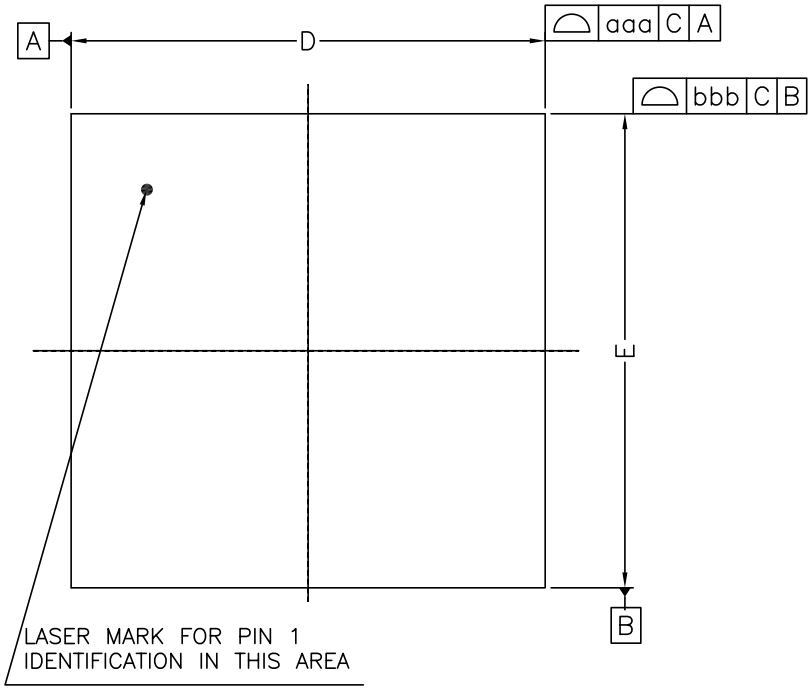
Pin #	Pin Name	I/O	Description
1	VSS	Power	Digital Ground
2	EEPROM_SCL	I	Serial Clock Input from external EEPROM load
3	EEPROM_SDA	I/O	Serial Data from external EEPROM load
4	NC		
5	NC		
6	VDD33	Power	3.3V analog power input
7	NC		
8	VDD33	Power	3.3V analog power input
9	LDO_CAP		Connect internal LDO to output capacitor
10	NC		
11	NC		
12	NC		
13	NC		
14	XRX_1	I	Accepts single ended clock 3.3V LVCMOS clock output
15	XRX_P	I	Accept XO or 3.3V LVPECL/LVDS positive clock output
16	XRX_N	I	Accept XO or 3.3V LVPECL/LVDS negative clock output
17	VDD_ANALOG	Power	3.3V analog power input
18	VSS_ANALOG	Power	Analog Ground
19	VDD_ANALOG	Power	3.3V analog power input
20	NC		
21	VDD_OUT1	Power	3.3V analog power input
22	OUT1_N	O	Differential output 1 negative (LVPECL/LVDS) or LVCMOS
23	Out1_P		Differential output 1 positive (LVPECL/LVDS) or LVCMOS
24	VDD_OUT2		3.3V analog power input
25	OUT2_N	O	Differential output 2 negative (LVPECL/LVDS) or LVCMOS
26	OUT2_P	O	Differential output 2 positive (LVPECL/LVDS) or LVCMOS
27	VDD_OUT3	Power	3.3V analog power input
28	OUT3_N	O	Differential output 3 negative (LVPECL/LVDS) or LVCMOS
29	OUT3_P	O	Differential output 3 positive (LVPECL/LVDS) or LVCMOS
30	VDD_OUT4	Power	3.3V analog power input
31	OUT4_N	O	Differential output 4 negative (LVPECL/LVDS) or LVCMOS
32	OUT4_P	O	Differential output 4 positive (LVPECL/LVDS) or LVCMOS
33	EPROM LOAD	I	Active high to load firmware via external EEprom into pins 2 and 3.
34	VDD_ANALOG	Power	Analog 3.3V power input
35	VDD_ANALOG	Power	Analog 3.3V power input
36	NC		
37	OUT5_P	O	Differential output 3 negative (LVPECL/LVDS) or LVCMOS
38	OUT5_N	O	Differential output 3 positive (LVPECL/LVDS) or LVCMOS
39	VDD_OUT5	Power	3.3V analog power input
40	OUT6_P	O	Differential output 4 negative (LVPECL/LVDS) or LVCMOS
41	OUT6_N	O	Differential output 4 positive (LVPECL/LVDS) or LVCMOS
42	VDD_OUT6	Power	3.3V analog power input
43	OUT7_P	O	Differential output 7 positive (LVPECL/LVDS) or LVCMOS
44	OUT7_N	O	Differential output 7 negative (LVPECL/LVDS) or LVCMOS
45	VDD_OUT7	Power	Analog 3.3V power input
46	OUT8_P	O	Differential output 8 positive (LVPECL/LVDS) or LVCMOS
47	OUT8_N	O	Differential output 8 negative (LVPECL/LVDS) or LVCMOS
48	VDD_OUT8	Power	Analog 3.3V power input
49	NC		
50	VDD_ANALOG	Power	Digital 3.3V power input

NC2008 Pin Assignments continued

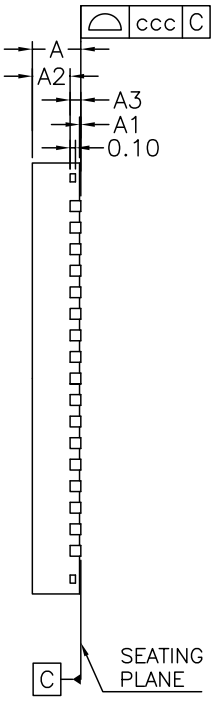
Pin #	Pin Name	I/O	Description
51	VSS_ANALOG	Power	Analog Ground
52	VDD_ANALOG	Power	3.3V power input YPLL2
53	YX0 or OUT9	0	Output of YRX_1 Signal or XTAL input pad
54	YX1 or YRX_1	I	Accept XO 3.3V LVCMOS clock output or XTAL Input pad
55	VDD_ANALOG	Power	3.3V power input YPLL2
56	NC		
57	NC		
58	NC		
59	NC		
60	RESET_N		Resets chip
61	NC		
62	NC		
63	NC		
64	VDD33	Power	Digital 3.3V power input
65	SDA	O	SPI bus data output
66	SCL	I	SPI bus data input
67	NC		
68	NC		

Pin Descriptions

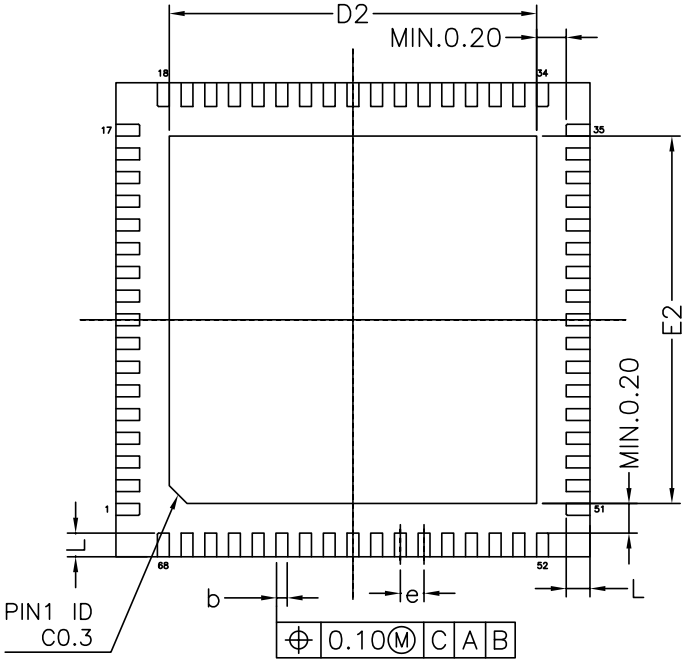
Mechanical Drawings



TOP VIEW



SIDE VIEW



BOTTOM VIEW

* CONTROLLING DIMENSION : MM

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	0.035	0.05	0.00	0.001	0.002
A2	---	0.65	0.67	---	0.026	0.026
A3	0.203 REF.			0.008 REF.		
b	0.15	0.20	0.25	0.006	0.008	0.010
D	7.90	8.00	8.05	0.311	0.315	0.317
D2	6.10	6.20	6.30	0.240	0.244	0.248
E	7.90	8.00	8.05	0.311	0.315	0.317
E2	6.10	6.20	6.30	0.240	0.244	0.248
L	0.35	0.40	0.45	0.014	0.016	0.018
e	0.40 bsc			0.016 bsc		
TOLERANCES OF FORM AND POSITION						
aaa	0.10			0.004		
bbb	0.10			0.004		
ccc	0.05			0.002		

Diagram 4: Package Dimensions

NC2008 Multi Output Clock Generator IC

CONNOR WINFIELD

Revision History

Revision	Revision Date	Note
00	09/20/17	Initial Release
01	03/25/19	Updated New Drawings - Block Diagram, Mechanical and Pins
02	07/22/20	Updated PLL information
03	01/05/21	Updated Model Name