NF2004 Synchronizing IC for Frequency Translation, Jitter Attenuation and Clock smoothing

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Overview

The NF2004 is a highly integrated synchronizing ASIC for applications that require frequency translation, low noise jitter attenuation, multi output clock generation and clock synthesis. The design implementation is intended to be flexible offering multiple configurations that can be used to optimize low noise frequency generation and/or frequency translation. The design architecture incorporates sophisticated analog PLL scheme which can provide up to 17 phase/frequency locked single ended output(s) or 8 differential (LVPECL or LVDS) outputs at frequencies from 1 kHz to 800 MHz. The NF2004 supports two reference inputs from single ended clock sources at frequencies from 8 kHz to 125MHz. Up to two external disciplined VCXOs provide the output characteristics for phase noise and jitter performance. The VCXO signals can be either passed through directly to eight programmable output transmitters, maintaining their low phase noise characteristics or they can support a second order high frequency PLL for clock synthesis via the NF2004's 20 bit divider capability at each output transmitter port. Output jitter performance, depending upon the configuration chosen, can achieve levels of 70fs RMS (12 kHz to 20MHz) for direct signal pass through or sub .3ps for synthesized clock outputs.

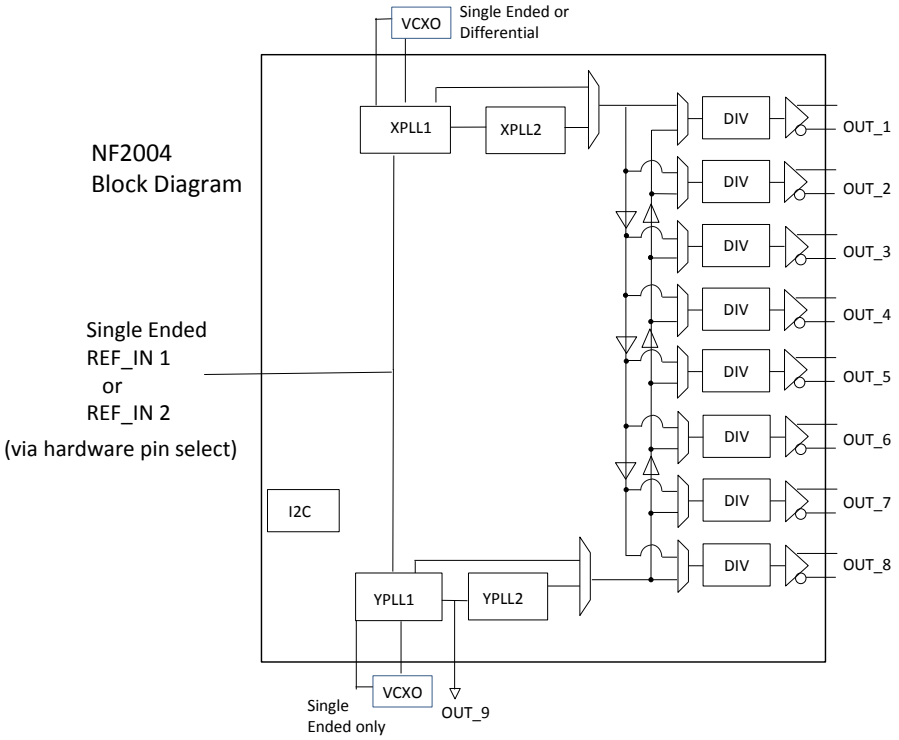
Features

- Two Reference inputs (each can accept one LVCMOS reference signal/ clock)
- 1 Hz to 800 MHz clock output frequency range
- Eight differential or up to 17 single ended Low Jitter Clock Outputs
- Programmable output transmitters (programmable as either 1 LVPECL, 1 LVDS or 2x LVCMOS output)
- Low jitter clock outputs (less than .3ps RMS (12kHz to 20MHz) with optional configurations for sub 100fs performance
- I2C Interface for system communica tion and interrogation.
- 8 x8 mm 68 pin QFN surface mount package

Typical Applications

- Frequency Translation
- Clock smoothing
- Jitter Attenuation
- Clock Generation
- Wireless Base Stations
- GNSS Disciplined Oscillator

NF2004 Functional Port Diagram



RoHS COMPLIANT

Bulletin	TM135
Revision	04
Date	12 Jan 2021

Specifications

Parameter	Specification
Voltage	3.3V ±5%
Power	Based on configuration (100ma with outputs tri-stated) Outputs add: LVPECL 50ma, LVDS 20Ma, LVCMOS 8 ma
Temperature	-40 to 85 C Industrial temp range operation
Reference Frequency	Single ended clock input 8KHz – 125MHz
Low Jitter Clock Output Frequency	1 Hz to 800 MHz
Dimensions	8 x 8x 1mm 68 pin QFN package

NF2004 General Description

The NF2004 is a highly integrated phase lock loop frequency translation and jitter attenuating ASIC. The design architecture incorporates a sophisticated analog PLL scheme to provide up to 17 phase locked clock outputs at frequencies from 1Hz to 800 MHz. The NF2004 can switch, via hardware pin, between two 3.3V LVCMOS reference input clock sources at frequencies from 8 kHz - 125MHz.

The NF2004 supports two independent frequency domains, each of which can be attenuated internally to ultra low jitter levels and multiple output clocks. The internal design architecture consists of two independent analog PLL chains (X side and Y side) that attenuate jitter initially through a first stage PLL. Offering a variety of optional configurations, the NF2004 offers direct pass through signals from the first stage PLL to the output transmitters or through a second stage high frequency PLL that synthesizes outputs that can be directly integer divided from the second stage PLL's VCO frequency. These options allow the user to achieve either low or ultra-low jitter performance levels from the eight programmable output transmitters. The output transmitters offer 3 in 1 programmability such that each transmitter can be programmed as either two (2) LVCMOS outputs, one (1) LVPECL output or one (1) LVDS output. The chip can operate using both X side and Y side analog PLLs to generate a combination of both X and Y side frequencies or all outputs can be supported from either the X or the Y side alone. One or two disciplined VCXO(s) provides the output characteristics for phase noise and jitter performance for the clock outputs. With minimal additive jitter from the ASIC, VCXOs with very low jitter (e.g. 50 fs) can be passed through directly to the output dividers/transmitters to provide output jitter performance of less than 80fs RMS over the integration range of 12 kHz to 20MHz, critical for today's wireless systems.

The NF2004 was designed to provide ultimate flexibility in achieving low jitter performance of its outputs. The two X-side and Y-side internal A-PLL chains are configured slightly differently from each other to make it a highly versatile frequency translator and jitter attenuator designed to meet requirements for multiple applications, including: clock generation and translation for SONET, 40G,100G and 400G Synchronous Ethernet network elements, clock distribution with low phase noise, and other applications demanding sub-picosecond jitter performance.

Reference Input Select (REF_SELECT)

The NF2004 is designed to accept two single ended 3.3V LVCMOS reference inputs. A REF_SELECT pin allows the user to manually switch between the two reference inputs, REF_IN1 and REF_IN2. Both X and Y sides of the analog APLL chains can lock to a single reference input at a time. Pin 67 provides the means to select between which reference is chosen to lock to. Applying GND to pin 67 will enable REF_IN1. Applying 3.3V to pin 67 will enable REF_IN2. Registers are available to adjust the divider to choose the appropriate phase detector frequency (PFD) required to support two different reference input frequencies.

NF2004 Analog PLL Chain Description

The NF2004 supports two independent analog PLL chains (X,Y) to support two simultaneous, independent frequency domains that share ten programmable clock output transmitter ports. There is an additional single ended output on the Y-side (Output 10). The NF2004 consists of two (2) independent sets of two (2) cascaded PLL stages, referred to as the X and the Y side. In each X and Y side of the chip, the first stage PLL (XPLL1 and YPLL1) attenuates the initial jitter from the reference input/NPLL with the use of an external VCXO.

When in operation, the locked VCXO signal can be sent directly to the output transmitter ports for a direct pass through of the VCXO frequency or further divided using the independent 20 bit divider circuits at each output transmitter port.

Alternatively, the VCXO frequency/signal can be sent to a second stage PLL. A second stage PLL for each X and Y side (XPLL2 and YPLL2) with an integrated high frequency VCO is available to accept the output of the first stage PLL1. Each PLL2 has an integrated phase frequency detector, charge pump and VCO in the usable range of 1.2GHz to 1.475 GHz that can be employed to generate locked output clocks at the eight output transmitter ports using the eight independent 20 bit divider circuits found at each transmitter ports.

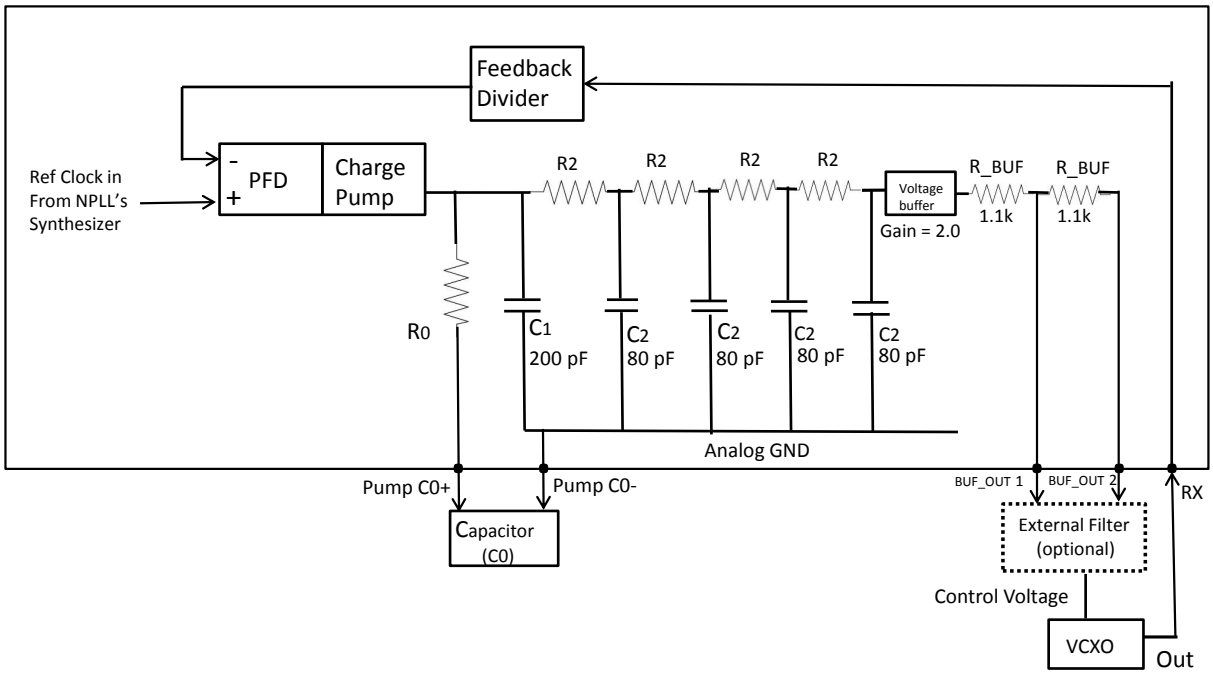
This design architecture gives the user a great deal of control over the output phase noise and jitter level generated by the NF2004. An external VCXO with exceptional phase noise and jitter performance can be used in bypass mode of the NF2004 to retain the ultra-low jitter performance characteristics with very little additive jitter contributed by the NF2004 . Low frequency VCXO sources (as low as 1 MHz) as well as differential clock sources (up to 800 MHz) can be used in bypass mode to achieve maximum jitter attenuation. If outputs are generated using PLL2, single ended VCXOs at frequencies between 40 MHz and 100 MHz should be used for best performance. Depending upon the external VCXO configuration used, clock outputs can be generated in the frequency range from 1Hz to 800MHz, limited to 180MHz for LVCMOS outputs.

PLL1 (X,Y) General Description

PLL1's (X,Y) function in the NF2004 it to act as a frequency translator and jitter attenuator. PLL1(X,Y) effectively attenuates the jitter from the incoming reference clock and translates the frequency to that of the chosen external VCXO which supports it. PLL1(X,Y) can pass through the external VCXO frequency directly to the output dividers and transmitters or be used as the input frequency to the second stage PLL, PLL2 (X,Y). When the VCXO clock output is passed directly through to the output dividers and transmitters, the NF2004 is capable of attenuating the jitter with approximately 10fs additive jitter to that of the external 3.3V VCXO.

PLL1(X,Y) consists of a phase-frequency detector (PFD), charge pump, passive loop filter, and an external VCXO operating in a closed loop. PLL1(X,Y) has the flexibility to operate with a loop bandwidth of approximately 10Hz to 200 Hz. This relatively narrow loop bandwidth gives it the ability to suppress jitter that appears on the synthesized clock signal feeding PLL1 from the NF2004 's NPLL. This synthesized clock eliminates the requirement for a phase detector frequency relationship between the frequency of the reference inputs into the NF2004 and the output VCXO frequency desired. The NPLL's synthesizer frequencies are programmable allowing for a flexible phase detector rate however the PFD rate must be divisible by 8kHz (8 kHz * M where <1 M <=5000). The charge pump current ,feedback divider, R0,and R2 are register programmable inside the chip. Capacitors C1 and C2 are internal and are fixed values. One external capacitor is required for the NF2004's loop filter, which connects to pins Pump_C0+ and Pump_C0- . An optional external filter on the control voltage pin of the external VCXO is supported through Buf_Out1 and Buf_Out2 pins.

PLL 1 Circuit Diagram (X , Y)

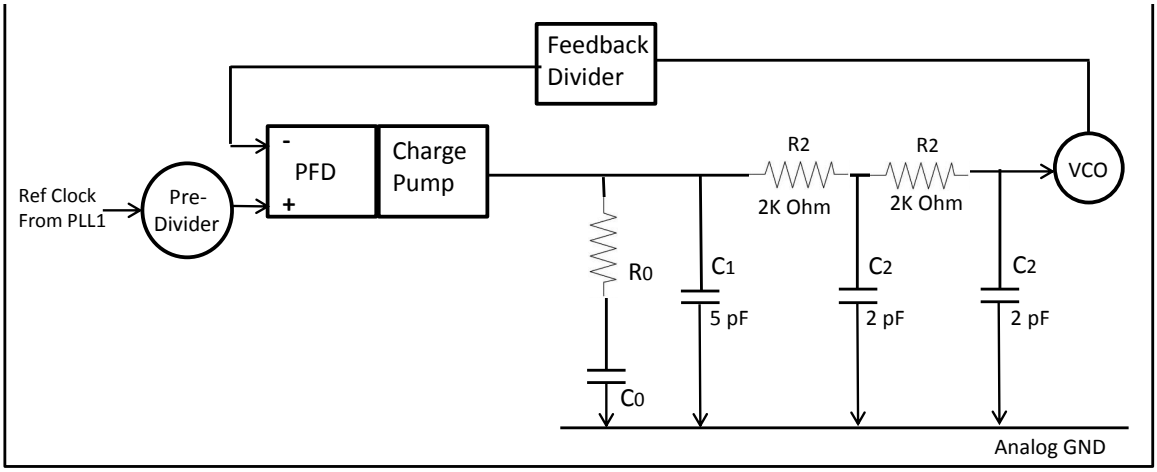


PLL2 (X, Y) General Description

PLL2 (X,Y) operates as a second stage analog PLL block, taking its reference input directly from PLL1 (X,Y). PLL2 (X,Y) consists of a fully integrated phase-frequency detector (PFD), charge pump, integrated loop filter, and integrated internal VCO operating in a closed loop. The NF2004 's internal VCO operates in the effective frequency range from 1.2GHz to 1.495GHz. Due to the wide range of frequency options of the VCXO input into PLL1 (X,Y), a pre-divider is made available for PLL2. The VCXO frequency used in PLL1 (X,Y) is usually used as the reference frequency into PLL2 (X,Y), however if the VCXO frequency used in PLL1 (X/Y) is greater than 180MHz, the PLL2 (X,Y) pre-divider should be used to keep the input frequency to PLL2 (X,Y) to less than 180 MHz. Once the input frequency into PLL2 (X,Y) has been determined, the appropriate feedback divider value should be chosen match the input frequency to the VCO frequency in the NF2004's usable range. When setting up the registers for PLL2 (X,Y), it is important to note that the values of the registers for setting up PLL1 (X,Y) and PLL2 (X,Y) should be completed and set, including pre-divider and feedback divider for PLL2 (X,Y) prior to initiating the X and Y PLL MODE register setting (0x05 and 0x06). This sequence of operation is required for an automatic self calibration necessary to ensure proper locking of PLL2 (X,Y) to the incoming reference signal from PLL1 (X,Y).

Once PLL2(X,Y) is properly locked, the chosen VCO frequency can be integer divided using the 20 bit programmable post-divider circuits preceding the programmable output transmitter ports. The charge pump current, feedback divider, R0, C0 and the Kvco of the internal VCO are register programmable inside the chip and can be updated/changed during operation after the PLL is locked successfully. Capacitors C1 and C2 and R1 are predefined fixed values.

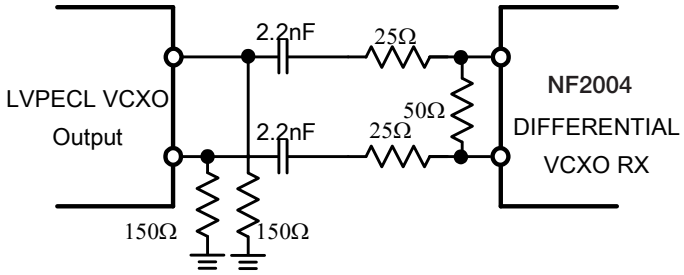
PLL2 Circuit Diagram (X, Y)

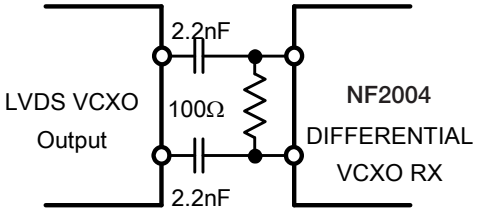


X-Side PLL Chain

On the X side of the chip, XPLL1 can be supported by a single ended or differential VCXO at frequencies from 10MHz to 800MHz.. Well-chosen high frequency VCXOs can provide jitter performance levels in the 50 to 60fs range and thus locked outputs from XPLL1 can provide well under 100fs jitter performance levels in the integration band of 12 kHz to 20MHz. This frequency can then be passed through to additional output transmitters/dividers and/or be used as an input to the second stage PLL (XPLL2) to synthesize additional output frequencies at the output transmitter ports. Outputs derived from XPLL2, depending upon frequency, will generally provide jitter performance levels of < 300fs over the integrated band of 12kHz to 20 MHz.

Differential VCXO termination recommendation in to pins XRX_P and XRX_N





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ADDR	NAME	TYPE	BITS	DEFAULT	DESCRIPTION
0x04	XPLL Mode	RW	2 - 0	0	XPLL Mode 0, 5, 6, 7: power down 1: PLL1 with single-end vcxo -> PLL2 2: PLL1 with differential vcxo -> PLL2 3: PLL1 only with single-end vcxo 4: PLL1 only with differential vcxo

Y-Side PLL Chain Description

On the Y side of the chip, YPLL1 can be supported by a single ended VCXO only at frequencies from 10MHz to 180MHz. At Output 9, the phase locked VCXO nominal frequency will bypass directly to Output 9 which offers an optimized clock jitter performance with the least additive jitter from the chip. Output 9 is LVCMOS only which effectively acts as a buffer from the VCXO in and directly out of the chip to achieve optimal jitter (usually less than 10fs additive jitter) for ultra-low jitter applications. A well-chosen high frequency LVCMOS VCXO can provide jitter performance levels in the 50-60 range and thus locked outputs from YPLL1 can provide well under 80fs jitter performance levels in the integration band of 12kHz to 20MHz. This VCXO clock frequency signal can then be “by-passed” through to additional output transmitters/dividers or be used as an input to the second stage PLL (YPLL2) to synthesize additional output frequencies at the output transmitter ports through the use of the 20 bit divider. Outputs derived from YPLL2, depending upon frequency, will generally provide jitter performance levels of < 300fs over the integration band of 12kHz to 20 MHz.

ADDR	NAME	TYPE	BITS	DEFAULT	DESCRIPTION
0x05	YPLL Mode	RW	0	0	YPLL Mode 0, 5, 6, 7: power down 1,2: PLL1 with single-end vcxo -> PLL2 3,4: PLL1 only with single-end vcxo

Eight 3-in-1 Programmable Output Transmitter Ports

Output transmitter ports 1 through output 8 consist of programmable 3-in-1 transmitters that can be configured to output either (2) LVCMOS or 1 LVDS or 1 LVPECL logic signal. Output transmitters can be powered down if not in use. When using LVCMOS mode, outputs can be generated on both output pins (P and N) of the output transmitter, or, one or the other. Polarity of the LVCMOS output at each pin is controllable.

ADDR	NAME	TYPE	BITS	DEFAULT	DESCRIPTION
0x31	Output1 Transmitter Mode	RW	4 - 0		Output1 transmitter mode, Bit[2:0] 0, 6, 7: power down, 1: LVDS 2: LVPECL 3: LVCMOS, P on, N off 4: LVCMOS, P off, N on 5: LVCMOS, P on, N on When transmitter is in LVCMOS mode, Bit[5:4] control polarity of output Bit4 0: P is not inverse, 1: P inverse Bit5 0: N is not inverse, 1: N is inverse

Output Transmitter Port Description

Output transmitter ports 1 through 8 are divided into four output “banks”. Each of the four output banks must be controlled as a unit. Bank0 (Output transmitters 1 and 2), Bank1 (Output transmitters 3 and 4), Bank2 (Output transmitters 5 and 6), and Bank3 (Output transmitters 7 and 8) represent four “banks” of outputs that can be controlled independently from each X and Y side of the chip. Either the X side or the Y side of the chip can access all four output banks, thus eliminating the requirement to use both sides X and Y in all applications. However, X and Y side clock signals must access output banks in order and must stop at the first output bank placed in use by the alternate side. For example, if X side uses banks 0, 1 and 2, Y side can only access bank 3 (outputs transmitters 7 and 8) or if Y side uses banks 3 and 2 (output transmitters 8,7 and 6,5), X side can only access bank 1 and 0 (outputs transmitters 1,2 and 3,4).

ADDR	NAME	TYPE	BITS	DEFAULT	DESCRIPTION
0x3b	Output Source Selection	RW	2 - 0	0	Output 1 ~ 8 source selection, output can come from either xpll or ypll, the arrangement are as follows, 0,5,6,7: xpll -> 1,2,3,4,5,6,7,8 1: xpll -> 1,2,3,4,5,6 ypll ->7,8 2: xpll -> 1,2,3,4 ypll -> 5,6,7,8 3:xpll -> 1,2 ypll -> 3,4,5,6,7,8 4:ypll -> 1,2,3,4,5,6,7,8

Output Bank Details and Constant Skew Delay Description

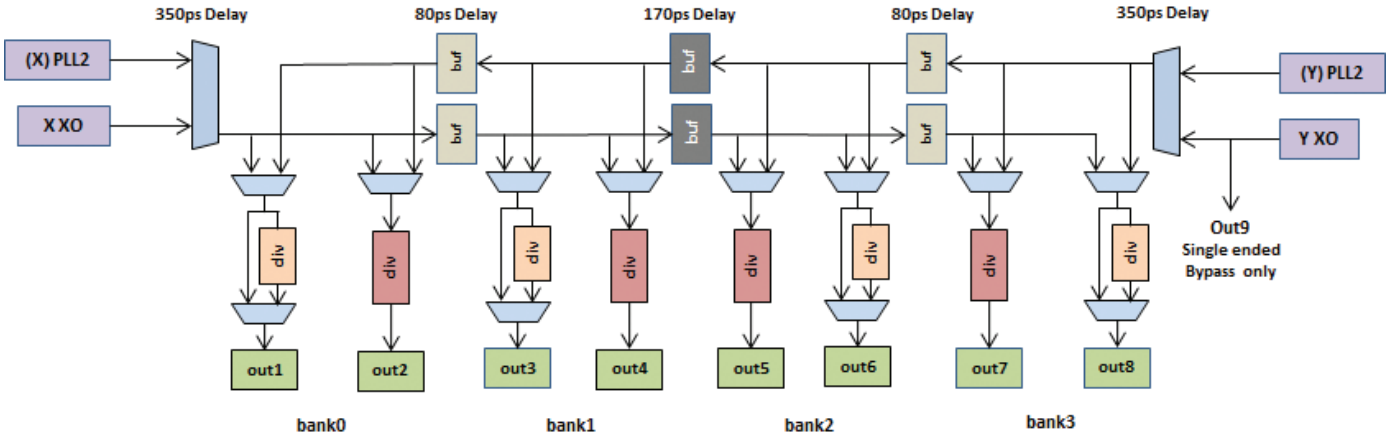


Diagram 1 Detailed Output Port Diagram

Output Skew Description

The skew between clock outputs is constant but will exhibit a cumulative delay relative to each other based on the clock signal traveling through MUXs and Buffers. This will be dependent upon how the output banks are configured from each X and Y side. Delay time are identified in Diagram 1.

20 bit Divider Circuits

Output ports 1-8 have 20 bit divider capability (any integer value from 1-1,048,576). Regardless if the frequency is generated by the VCO or if it is bypassed through from the reference input source, the divider circuit can be used to generate divided frequencies. For instance, using a 1MHz input clock source in bypass mode, can achieve a 1Hz output through the divider circuit. Please note, low frequency input options are only available in bypass mode as inputs to the X and Y PLL requires a minimum of 40 MHz input frequency.

ADDR	NAME	TYPE	BITS	DEFAULT	DESCRIPTION
0x40 ~ 0x42	Output 1 Divider Value	RW	19 - 0	0	20 bit OUTPUT1 divider value

Symmetry Control for low value odd dividers

Output transmitter circuit numbers 2, 4, 5 and 7 have, by default, output symmetry control when dividing by a single digit, odd integer value. In circumstances which require dividing the VCO output frequency by values of 3, 5, 7 or 9, one of these output transmitter circuits should be used to achieve 50/50 duty cycle. When using an odd divider value of greater than nine (9), symmetry control is generally not required to maintain reasonable symmetry in the output. The output ports offering symmetry control do not allow for a direct by-pass through of the reference input frequency and require dividing at the output transmitter circuit by a minimum by 2. Output ports 1, 3, 6 and 8 can by-pass the divider circuit entirely or can divide by any integer number up to the 20bit value.

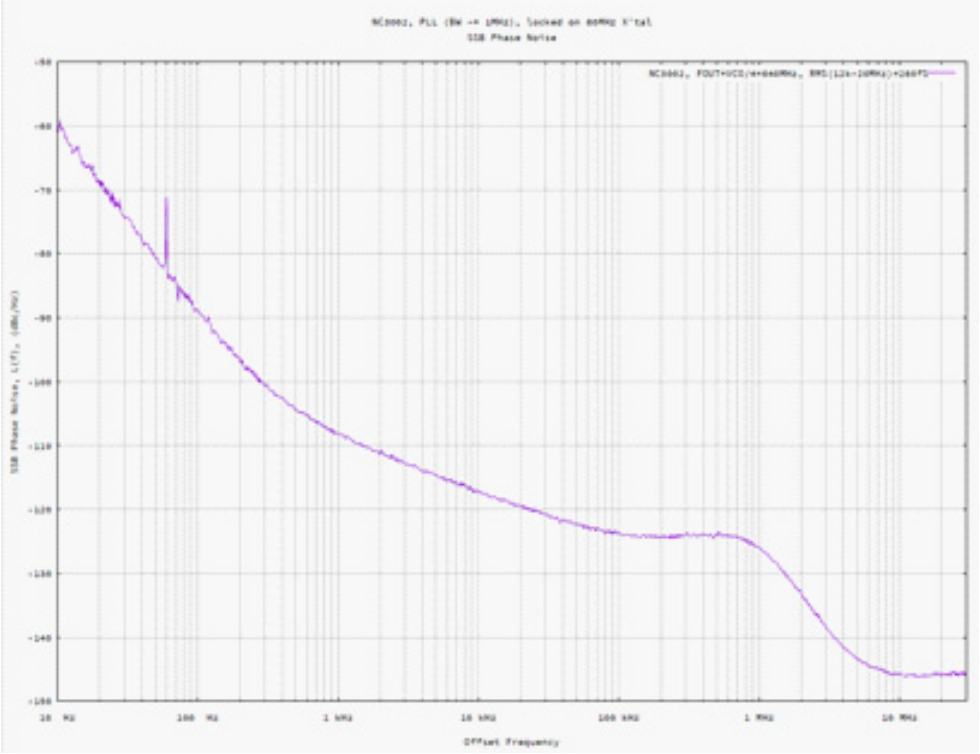
Layout Recommendations

The printed circuit board that houses the NF2004 should be designed so that the analog and digital sections are separated and confined to certain areas of the board. This facilitates the use of ground planes that can be easily separated. A minimum etch technique is generally best for ground planes because it gives the best shielding. Digital and analog ground planes should be joined in only one place. If the NF2004 is the only device requiring an AGND-to-DGND connection, then the ground planes should be connected at the AGND and DGND pins of the NF2004. If the NF2004 is in a system where multiple devices require AGND-to-DGND connections, the connection should be made at one point only, a star ground point that should be established as close as possible to the NF2004.

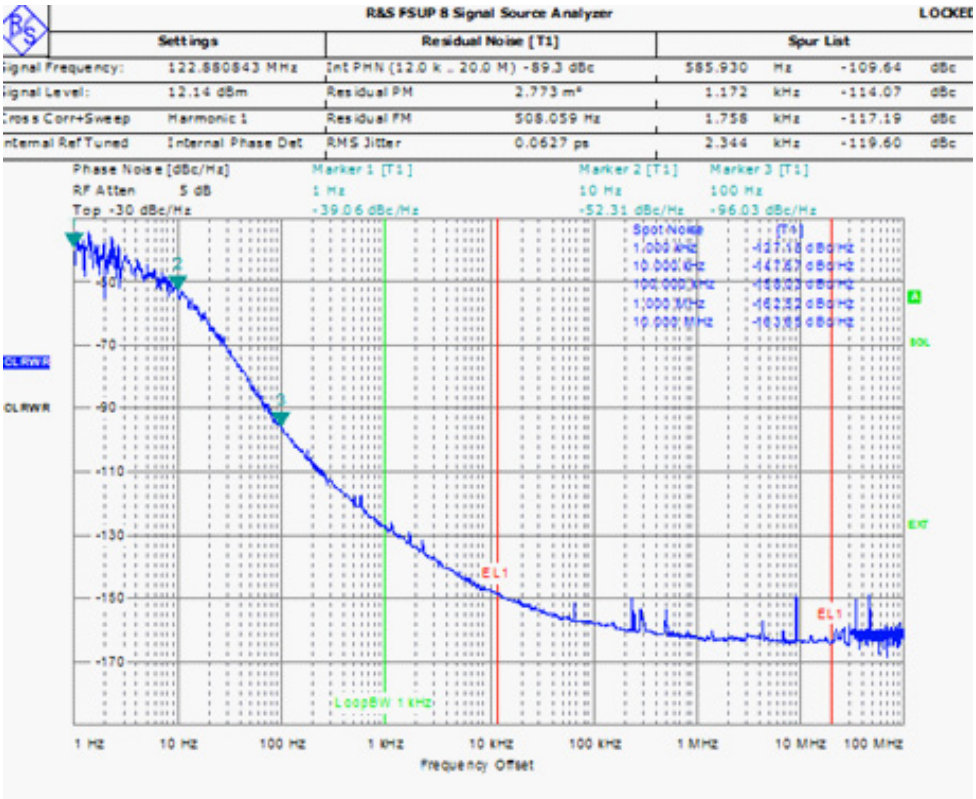
Avoid running digital lines under the device because these couple noise onto the die. The analog ground plane should run under the NF2004 to avoid noise coupling. The power supply lines to the NF2004 should use as large a track as possible to provide low impedance paths and reduce the effects of glitches on the power supply line. Fast switching signals, such as clocks, should be shielded with digital ground to avoid radiating noise to other sections of the board. Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other, reducing the effects of feed-through. A micro-strip technique is by far the best but is not always possible with a double-sided board. In this technique, the component side of the board is dedicated to ground planes, while signals are placed on the other side.

Good decoupling is important. The analog and digital supplies to the NF2004 are independent and separately pinned out to minimize coupling between analog and digital sections of the device. All analog and digital supplies should be decoupled to AGND and DGND, respectively, with 0.1 µF ceramic capacitors in parallel with 10 µF tantalum capacitors. To achieve the best from the decoupling capacitors, they should be placed as close as possible to the device, ideally right up against the device. In systems where a common supply is used to drive both the AVDD and DVDD of the NF2004, it is recommended that the system's AVDD supply be used. This supply should have the recommended analog supply decoupling between the AVDD pin of the NF2004 and AGND and the recommended digital supply decoupling capacitors between the DVDD pin and DGND.

Output Phase Noise Characteristics Examples

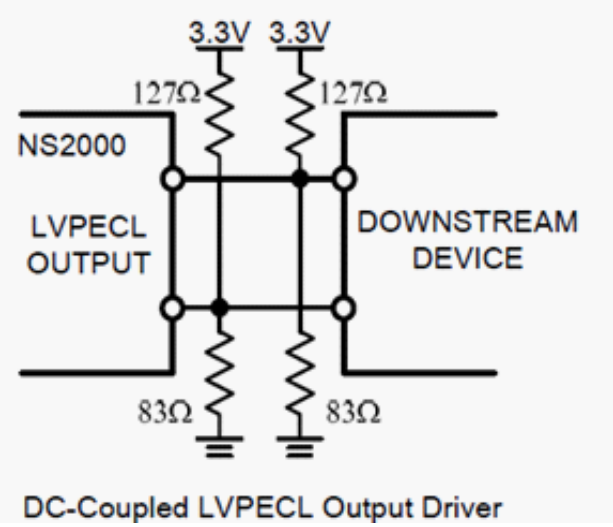


Phase noise generated from PLL2: 640MHz using 80MHz VCXO
260fs (12kHz-20MHz)

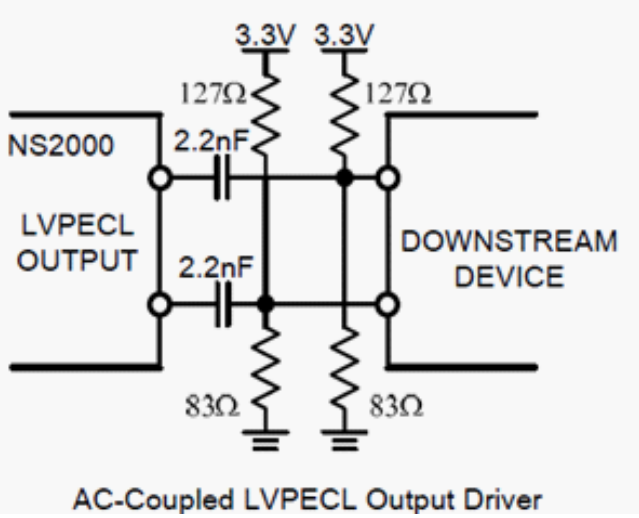


Phase noise generated from PLL1(y): 122.88MHz 63fs (12kHz-20MHz)
(using Connor Winfield model V773T-122.88MHz LVCMOS 5x3.2mm VCXO)

LVPECL Suggested Termination



DC-Coupled LVPECL Output Driver



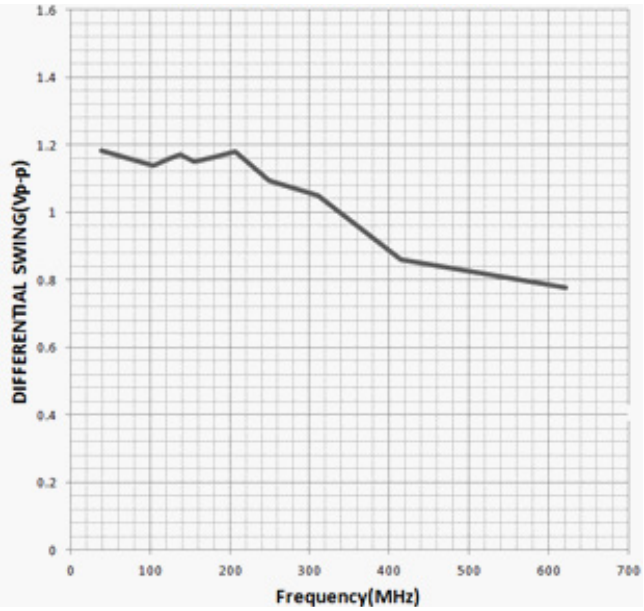
AC-Coupled LVPECL Output Driver

LVPECL Current Consumption

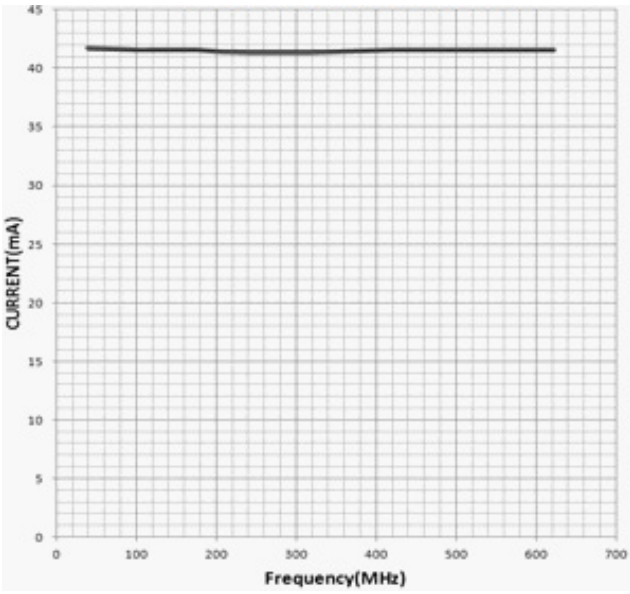
fvco=1.244GHz, fvcxo=38.88MHz,ftcxo=20MHz

OUTPUT FREQUENCY (MHz)	DUTY CYCLE (%)	RISE TIME (20%~80%)(ps)	CURRENT CONSUMPTION (mA)	DIFFERENTIAL SWING (Vp-p)
38.88	50.09	590	41.69	1.183
103.681	49.97	570	41.59	1.139
113.108	45.44	560	41.59	1.148
124.417	49.98	570	41.57	1.161
138.239	44.49	520	41.53	1.171
155.519	49.98	530	41.56	1.152
177.74	43.06	570	41.56	1.163
207.362	50.1	510	41.41	1.182
248.836	42	430	41.34	1.095
311.054	50.14	500	41.32	1.049
414.736	35.64	370	41.53	0.86
622.115	51.05	270	41.56	0.778

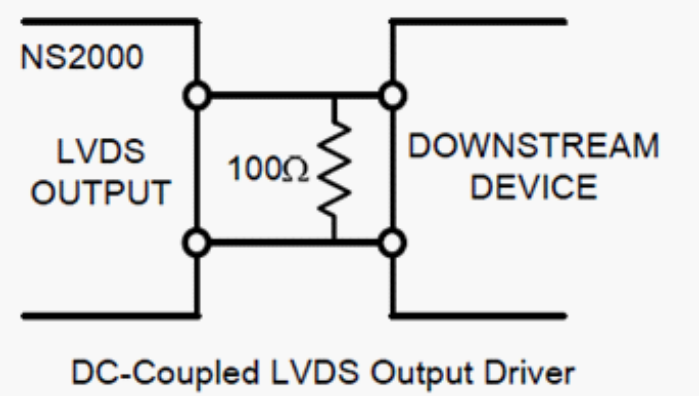
LVPECL Differential Swing



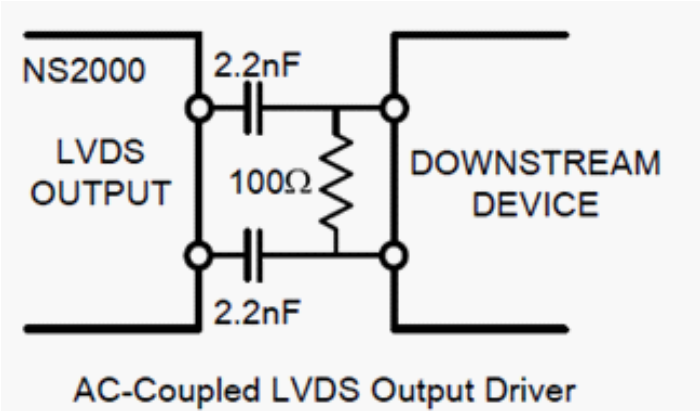
LVPECL Current Consumption



LVDS Suggested Termination



DC-Coupled LVDS Output Driver



AC-Coupled LVDS Output Driver

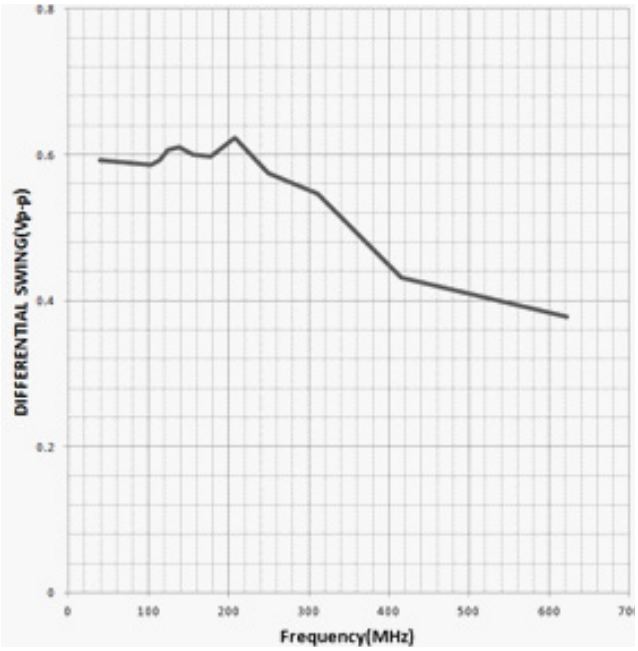
LVDS Current Consumption

fvco=1.244GHz, fvcxo=38.88MHz,ftcxo=20MHz

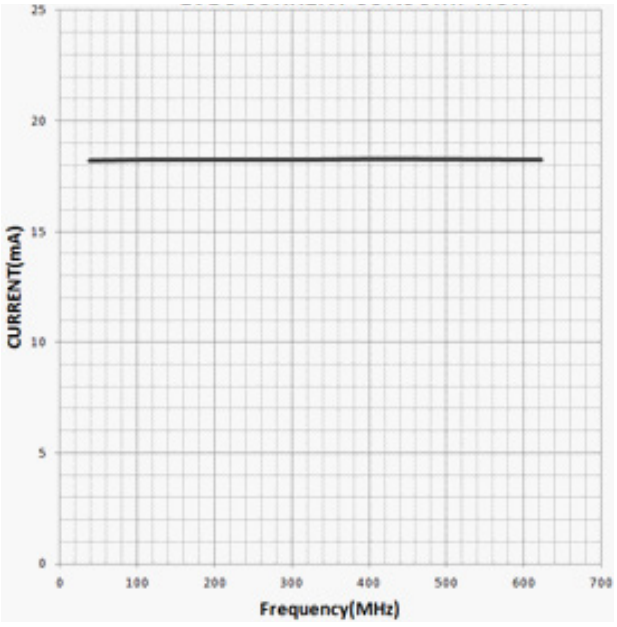
OUTPUT FREQUENCY (MHz)	DUTY CYCLE (%)	RISE TIME (20%~80%)(ps)	CURRENT CONSUMPTION (mA)	DIFFERENTIAL SWING (Vp-p)
38.8815	49.97	700	18.18	0.593
103.68	50.18	620	18.26	0.586
113.107	50.46	600	18.26	0.593
124.414	50.21	610	18.26	0.606
138.241	50.52	580	18.26	0.61
155.52	50.26	600	18.26	0.6
177.737	50.81	610	18.26	0.598
207.363	50.52	600	18.25	0.623
248.832	50.8	450	18.25	0.575
311.05	50.62	580	18.26	0.547
414.733	49.57	250	18.27	0.431
622.108	50.9	220	18.24	0.378

LVDS Output Common-Mode Voltage = 1.27V

LVDS Differential Swing



LVDS Current Consumption



NF2004 Register Table

ADDR	NAME	TYPE	BITS	DEFAULT	DESCRIPTION
0x00 ~ 0x01	Chip ID	RO	15 - 0	0x2004	Chip ID, it reflects the current product ID,
0x02	Chip Revision	RO	7 - 0	2	Chip Revision
0x03	Chip Sub-Revision	RO	7 - 0	1	Chip Sub revision
0x04	XPLL Mode	RW	2 - 0	0	XPLL Mode 0, 5, 6, 7: power down 1: PLL1 with single-end vcxo -> PLL2 2: PLL1 with differential vcxo -> PLL2 3: PLL1 only with single-end vcxo 4: PLL1 only with differential vcxo
0x05	YPLL Mode	RW	2 - 0	0	YPLL Mode 0, 5, 6, 7: power down 1,2: PLL1 with single-end vcxo -> PLL2 3,4: PLL1 only with single-end vcxo
0x06 0x07	REF1 Divider Value	RW	14 - 0	0	REF1 divider value for REF1 to PLL1 pfd frequency
0x08 ~ 0x09	REF2 Divider Value	RW	14 - 0	0	REF2 divider value for REF2 to PLL1 pfd frequency
0x10 0x11	XPLL1 FB Divider Value	RW	15 - 0	0	XPLL1 feedback divider value
0x12	XPLL1 R0 Range Selection	RW	0	0	XPLL1 R0 range selection, 0: Selection in Reg 0x14 1: Selection in Reg 0x13
0x13	XPLL1 R0 Value Selection0	RW	4 - 0	0	XPLL1 R0 value when reg0x12 == 0 Bit0, 0: 0.4k, 1: 2.5k Bit1, 0: 0.4k, 1: 5k Bit2: 0: 0.4k, 1: 10k Bit3: 0: 0.4k, 1: 20k Bit4, 0: 0.4k, 1: 40k
0x14 ~ 0x15	XPLL1 R0 Value Selection1	RW	8 - 0	0	XPLL1 R0 value when reg0x12 == 1 Bit0, 0: 1k, 1: 10k Bit1, 0: 1k, 1: 20k Bit2: 0: 1k, 1: 40k Bit3: 0: 1k, 1: 80k Bit4, 0: 1k, 1: 160k Bit5, 0: 1k, 1: 320k Bit6, 0: 1k, 1: 640k Bit7, 0: 1k, 1: 1280k Bit8, 0: 1k, 1: 2560k
0x16	XPLL1 R2 Value	RW	3 - 0	1	XPLL1 R2 Value 160k/reg_value
0x17 ~ 0x18	XPLL1 Charge Pump Current	RW	11 - 0	100	XPLL1 charge pump current Reg_value x 0.3125 uA
0x19	XPLL2 Pre Divider Value	RW	2 - 0	0	XPLL2 pre divider value
0x1a	XPLL2 FB Divider Value	RW	6 - 0	0	XPLL2 feedback divider value
0x1b	XPLL2 KVCO	RW	0	0	XPLL2 kvco 0: small 1: large

NF2004 Register Table continued

ADDR	NAME	TYPE	BITS	DEFAULT	DESCRIPTION
0x1c	XPLL2 C0 Value	RW	0	0	XPLL2 C0 value 0: 100 pF 1: 200 pF
0x1d	XPLL2 R0 Value	RW	3 - 0	0	XPLL2 R0 Value 0: 3k, 1: 4.2k, 2: 6k, 3: 8.4k, 4:12k, 5: 16.8k, 6: 12k, 7: 16.8k 8: 24k, 9: 33.6k, 10: 24k, 11: 33.6k , 12: 46.3k, 13: 66k, 14: 46.3k, 15: 66k
0x1e ~ 0x1f	XPLL2 Charge Pump Current	RW	10 - 0	100	XPLL2 charge pump current value, 1.25uA x reg_value
0x20 ~ 0x21	YPLL1 FB Divider Value	RW	15 - 0	0	YPLL1 feedback divider value
0x22	YPLL1 R0 Range Selection	RW	0	0	YPLL1 R0 range selection, 0: Selection in Reg 0x14 1: Selection in Reg 0x13
0x23	YPLL1 R0 Value Selection0	RW	4 - 0	0	YPLL1 R0 value when reg0x12 == 0 Bit0, 0: 0.4k, 1: 2.5k Bit1, 0: 0.4k, 1: 5k Bit2: 0: 0.4k, 1: 10k Bit3: 0: 0.4k, 1: 20k Bit4, 0: 0.4k, 1: 40k
0x24 ~ 0x25	YPLL1 R0 Value Selection1	RW	8 - 0	0	YPLL1 R0 value when reg0x12 == 1 Bit0, 0: 1k, 1: 10k Bit1, 0: 1k, 1: 20k Bit2: 0: 1k, 1: 40k Bit3: 0: 1k, 1: 80k Bit4, 0: 1k, 1: 160k Bit5, 0: 1k, 1: 320k Bit6, 0: 1k, 1: 640k Bit7, 0: 1k, 1: 1280k Bit8, 0: 1k, 1: 2560k
0x26	YPLL1 R2 Value	RW	3 - 0	1	YPLL1 R2 Value 160k/reg_value
0x27 ~ 0x28	YPLL1 Charge Pump Current	RW	11 - 0	100	YPLL1 charge pump current Reg_value x 0.3125 uA
0x29	YPLL2 Pre Divider Value	RW	2 - 0	0	YPLL2 pre divider value
0x2a	YPLL2 FB Divider Value	RW	6 - 0	0	YPLL2 feedback divider value
0x2b	YPLL2 KVCO	RW	0	0	YPLL2 kvco 0: small 1: large
0x2c	YPLL2 C0 Value	RW	0	0	YPLL2 C0 value 0: 100 pF
					1: 200 pF
0x2d	YPLL2 R0 Value	RW	3 - 0	0	YPLL2 R0 Value 0: 3k, 1: 4.2k, 2: 6k, 3: 8.4k, 4:12k, 5: 16.8k, 6: 12k, 7: 16.8k 8: 24k, 9: 33.6k, 10: 24k, 11: 33.6k , 12: 46.3k, 13: 66k, 14: 46.3k, 15: 66k
0x2e ~ 0x2f	YPLL2 Charge Pump Current	RW	10 - 0	100	YPLL2 charge pump current value, 1.25uA x reg_value

NF2004 Register Table continued

ADDR	NAME	TYPE	BITS	DEFAULT	DESCRIPTION
0x31	Output1 Transmitter Mode	RW	4 - 0		Output1 transmitter mode, Bit[2:0] 0, 6, 7: power down, 1: LVDS 2: LVPECL 3: LVCMOS, P on, N off 4: LVCMOS, P off, N on 5: LVCMOS, P on, N on When transmitter in LVCMOS mode, Bit[5:4] control polarity of output Bit4 0: P is not inverse, 1: P inverse Bit5 0: N is not inverse, 1: N is inverse
0x32	Output2 Transmitter Mode	RW	4 - 0	0	Same as Output1 Transmitter Mode
0x33	Output3 Transmitter Mode	RW	4 - 0	0	Same as Output1 Transmitter Mode
0x34	Output4 Transmitter Mode	RW	4 - 0	0	Same as Output1 Transmitter Mode
0x35	Output5 Transmitter Mode	RW	4 - 0	0	Same as Output1 Transmitter Mode
0x36	Output6 Transmitter Mode	RW	4 - 0	0	Same as Output1 Transmitter Mode
0x37	Output7 Transmitter Mode	RW	4 - 0	0	Same as Output1 Transmitter Mode
0x38	Output8 Transmitter Mode	RW	4 - 0	0	Same as Output1 Transmitter Mode
0x39	XPLL Output Source	RW	0	1	XPLL output source 0: XPLL1 1: XPLL2
0x3a	YPLL Output Source	RW	0	1	YPLL output source 0: YPLL1 1: YPLL2
0x3b	Output Source Selection	RW	2 - 0	0	Output 1 ~ 8 source selection, output can come from either xpll or ypll, the arrangement are as follows, 0,5,6,7: xpll -> 1,2,3,4,5,6,7,8 1: xpll -> 1,2,3,4,5,6 ypll ->7,8 2: xpll -> 1,2,3,4 ypll -> 5,6,7,8 3: xpll -> 1,2 ypll -> 3,4,5,6,7,8 4: ypll -> 1,2,3,4,5,6,7,8
0x40 ~ 0x42	Output1 Divider Value	RW	19 - 0	0	20 bit OUTPUT1 divider value
0x43 ~ 0x45	Output2 Divider Value	RW	19 - 0	0	20 bit OUTPUT2 divider value
0x46 ~ 0x48	Output3 Divider Value	RW	19 - 0	0	20 bit OUTPUT3 divider value
0x49 ~ 0x4b	Output4 Divider Value	RW	19 - 0	0	20 bit OUTPUT4 divider value
0x4c ~ 0x4e	Output5 Divider Value	RW	19 - 0	0	20 bit OUTPUT5 divider value
0x4f ~ 0x51	Output6 Divider Value	RW	19 - 0	0	20 bit OUTPUT6 divider value
0x52 ~ 0x54	Output7 Divider Value	RW	19 - 0	0	20 bit OUTPUT7 divider value
0x55 ~ 0x57	Output8 Divider Value	RW	19 - 0	0	20 bit OUTPUT8 divider value

Package Outline

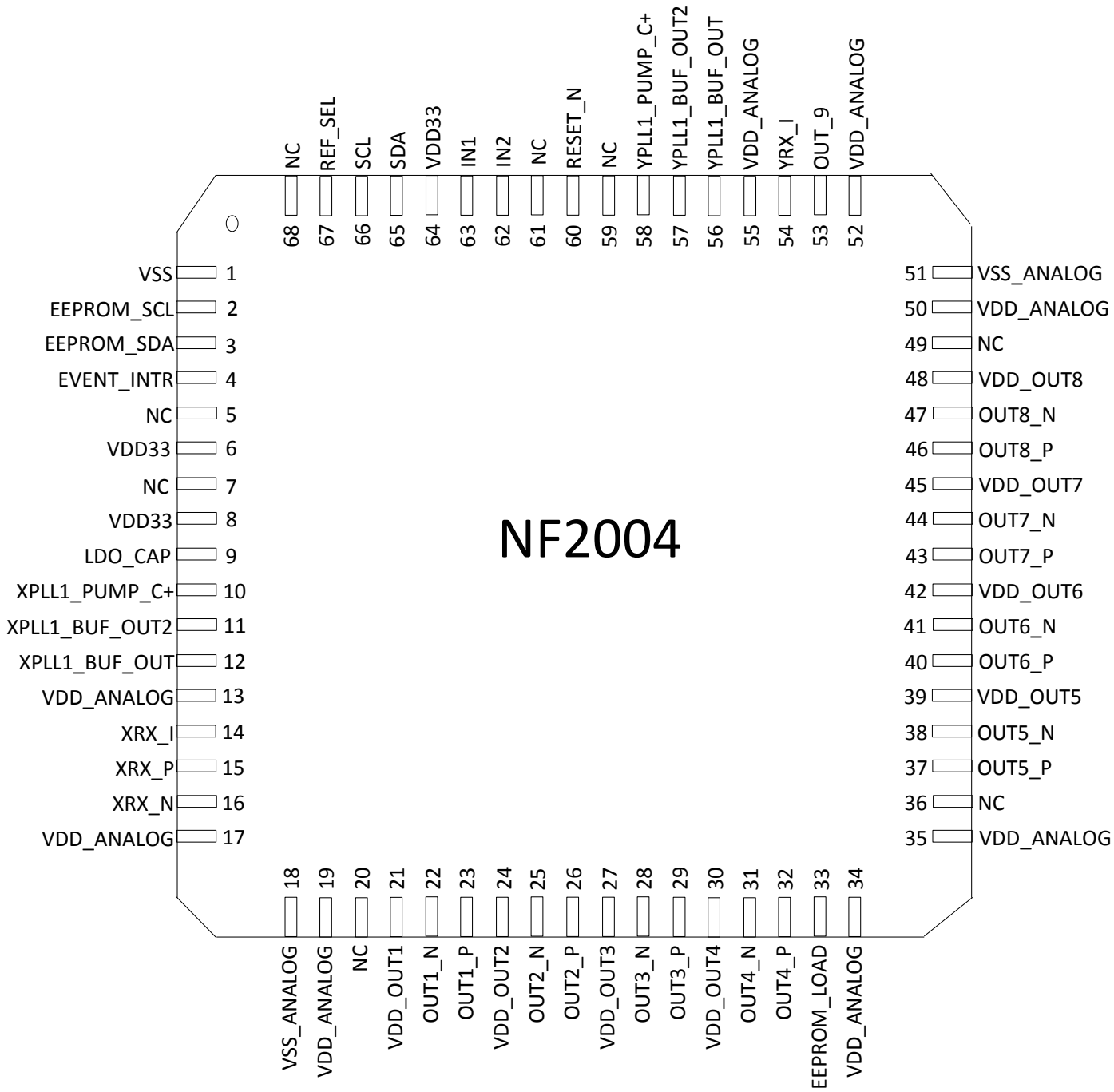


Diagram 2: Pin Out Map

NF2004 Pin Assignments

Pin #	Pin Name	I/O	Description
1	VSS	Power	Digital Ground
2	EEPROM_SCL	I	Serial Clock Input
3	EEPROM_SDA	I/O	Serial Data
4	NC		
5	NC		
6	VDD33	Power	3.3V digital power input
7	NC		
8	VDD33	Power	3.3V digital power input
9	LDO_CAP		Connect internal LDO to output capacitor
10	XPLL1_PUMP_C+		Connect to APLL's external filter +
11	XPLL1_BUF_OUT2		Connect to VCXO voltage control pin (optional connecting to cap)
12	XPLL1_BUF_OUT		Connect to VCXO voltage control pin (optional connecting to cap)
13	VDD_ANALOG	Power	3.3V analog power input)
14	XRX_1	I	Accept XO or VCXO's 3.3V LVCMOS clock output 3.3V analog power input
15	XRX_P	I	Accept XO or VCXO's 3.3V Differential (P) clock output 3.3V analog power input
16	XRX_N	I	Accept XO or VCXO's 3.3V Differential (N)clock output 3.3V analog power input
17	VDD_ANALOG	Power	3.3V analog power input
18	VSS_ANALOG	Power	Analog ground
19	VDD_ANALOG	Power	3.3V analog power input
20	NC		
21	VDD_OUT1	Power	3.3V analog power input
22	OUT1_N	O	Differential output 1 negative (LVPECL/LVDS) or LVCMOS
23	OUT1_P	O	Differential output 1 positive (LVPECL/LVDS) or LVCMOS
24	VDD_OUT2	Power	3.3V analog power input
25	OUT2_N	O	Differential output 2negative (LVPECL/LVDS) or LVCMOS
26	OUT2_P	O	Differential output 2 positive (LVPECL/LVDS) or LVCMOS
27	VDD_OUT3	Power	3.3V analog power input
28	OUT3_N	O	Differential output 3 negative (LVPECL/LVDS) or LVCMOS
29	OUT3_P	O	Differential output 3 positive (LVPECL/LVDS) or LVCMOS
30	VDD_OUT4	Power	3.3V analog power input
31	OUT4_N	O	Differential output 4 negative (LVPECL/LVDS) or LVCMOS
32	OUT4_P	O	Differential output 4 positive (LVPECL/LVDS) or LVCMOS
33	EEPROM_LOAD	I	Reset pin
34	VDD_ANALOG	Power	3.3V analog power input
35	VDD_ANALOG	Power	3.3V analog power input
36	NC		
37	OUT5_P	O	Differential output 5 positive (LVPECL/LVDS) or LVCMOS
38	OUT5_N	O	Differential output 5 negative (LVPECL/LVDS) or LVCMOS
39	VDD_OUT5	Power	3.3V analog power input
40	OUT6_P	O	Differential output 6 positive (LVPECL/LVDS) or LVCMOS
41	OUT6_N	O	Differential output 6 negative (LVPECL/LVDS) or LVCMOS
42	VDD_OUT6	Power	3.3V analog power input
43	OUT7_P	O	Differential output 7 positive (LVPECL/LVDS) or LVCMOS
44	OUT7_N	O	Differential output 7 negative (LVPECL/LVDS) or LVCMOS
45	VDD_OUT7	Power	3.3V Analog power input
46	OUT8_P	O	Differential output 8 positive (LVPECL/LVDS) or LVCMOS
47	OUT8_N	O	Differential output 8 negative (LVPECL/LVDS) or LVCMOS
48	VDD_OUT8	Power	3.3V Analog power input

NF2004 Pin Assignments continued

Pin #	Pin Name	I/O	Description
49	NC		No connection
50	VDD_ANALOG	Power	3.3V Analog power input
51	VSS_ANALOG	Power	Analog ground
52	VDD_ANALOG	Power	3.3V Analog power input
53	OUT9	O	LVCMOS 3.3V clock output direct from VCXO
54	YRX_1	I	Accept VCXO's 3.3V LVCMOS clock output
55	VDD_ANALOG	Power	3.3V Analog power input
56	YPLL1_BUF_OUT		Connect to VCXO voltage control pin (optional connecting to cap)
57	YPLL1_BUF_OUT2		Connect to VCXO voltage control pin (optional connecting to cap)
58	YPLL1_PUMP_C+		Connect to APLL's external filter +
59	NC		LVCMOS 3.3V clock output direct from VCXO
60	RESET_N		Resets Chip
61	NC		No connection
62	IN2	I	Reference Input 2, SIngle ended 3.3V LVCMOS input
63	IN1	I	Reference Input 1, SIngle ended 3.3V LVCMOS input
64	VDD33	Power	3.3V Digital Power Input
65	I2C_SDA	I	I2C Serial Data
66	I2C_SCL	I	I2C Serial Clock
67	REF_SELECT	I	REF_IN1 and REF_IN2
68	NC		

Pin Descriptions

Notes on Pin Description

RESET_N

Pin RESET_N is an I/O input pin used to initiate a “hard” reset to the IC. The RESET_N pin is internally “pulled-high”. Driving this pin “Low” for at least 1uS and releasing it, or driving it “High” again will reset the device. The IC will be ready to access through the control bus interface in 10 mS after the reset operation.

In addition to the RESET_N hardware pin reset function, a SOFT_RESET reboot option exists in the IC’s internal design. The register “SOFT_RESET” at 0 xA5 is a write-only register. Similar to the hard reset, once the register is written to, the IC’s registers will be ready to access through the control bus interface after 10mS.

Both the hard reset and the soft reset will cause the IC to reboot. The reboot procedure will first reload the content from the internal OTP. If the EEPROM_LOAD pin is tied “high”, an external EEPROM’s content will be loaded into the IC after the OTP content is loaded. Only the hard reset procedure will check the MCLK_RATE0 and MCLK_RATE1 to determine the clock frequency of the MCLK input.

This IC has a built-in power-on-reset (POR) circuit. However, a hard reset may need to be initiated if the supplied voltage to the IC has a very slow rising rate.

EEPROM_LOAD

EEPROM OPERATION: This IC supports the use of an external EEPROM to load firmware or default values of all read/write registers. This function is intended primarily to provide the ability for “field upgrade” flexibility to update firmware (Code+Data). Using an external EEPROM may also be considered for loading the default values of the read/write registers in preference to using the OTP memory. However, EEPROM content cannot be used to change the default values of read-only registers. CRC16 checksum protection is supported.

EEPROM BOOTING: The IC will always boot from the internal OTP content first. If the pin EEPROM_LOAD is tied “HIGH”, the IC will continue to download content from the EEPROM to override the OTP’s content during the boot-up stage. This procedure will be triggered after both a power cycle and a reset procedure (Hard or Soft).

EEPROM CONNECTION: This IC has an I2C master control dedicated to read/write data from a specific I2C EEPROM. The ATMEL AT24C256C (256-kbit I2C EEPROM IC) is required for use with this IC. For connection:

EEPROM’s I2C address ended with 0b000
- Ties pin A0, A1, A2 to ground

Disable write protection
- Ties pin WP to ground

Connect to this IC
- Tie pin SCL to this IC’s pin EEPROM_SCL
- Tie pin SDA to this IC’s pin EEPROM_SDA
- Data rate will be 1MHz (if traces are too long, some termination may be required)

EEPROM UPDATE OPERATION FROM USERS: This IC supports I2C bus interface as a control interface. This means the user can read/write content from/to the external EEPROM from this IC.

The EEPROM operations registers on this IC are:
- REG (EE_STS)
- REG (EE_PAGE_IDX)
- REG (EE_FIFO)
- REG (EE_CMD)

EEPROM content image
- Image size = 18,048 bytes
- Image content will be provided by manufacturer
- Each EEPROM image will be presented by an 18,048-byte long binary file
- Image integrity is protected by industry-grad CRC16 checksum

EEPROM Read/Write Operation
- Both read/write operation is in 64-byte page orientation
- The 18,048-byte binary image will be separated into 282 64-byte pages, indexed from 0 to 281

Page WRITE operation example:
- Wait until EE_STS indicates it is “ready”
- Setup the corresponding page index
- Issue FIFO pointer reset command
- Issue FIFO-read-from-EEPROM command
- Wait until EE_STS indicates it is ready
- Read the 64 byte page content from the FIFO port, in the order from LSB byte
- After updating the EEPROM content, read them back to ensure no corrupt data was generated during the read/write operation.

Notes on Pin Description continued

EEPROM_LOAD continued

Page READ operation example:

- Wait until EE_STS indicates IC is “ready”
- Setup the corresponding page index
- Issue FIFO pointer reset command
- Issue FIFO-read-from-EEPROM command
- Wait until EE_STS indicates IC is ready
- Read the 64 byte page content from the FIFO port, in the order from LSB to MSB byte
- After updating the EEPROM content, read them back to ensure no corrupt data was generated during the read/write operation.

CONTROL -BUS OPERATION

The control bus type of this IC uses a standard I2C interface. The I2 C interface has the advantage of requiring only two control pins and is a de facto standard throughout the I2C industry. The I2C port consists of a serial data line (SDA) and a serial clock line (SCL). In an I2C bus system, the NF2004 is connected to the serial bus (data bus SDA and clock bus SCL) as a slave device; that is, no clock is generated by the NF2004. The NF2004 uses direct 8-bit memory addressing.

Users can read/write registers through this control bus. The I2C slave controller does not support multi-master operation. Supporting clock rate is up to 1MHz.

The fixed I2C address is: Slave address = 0b101.0001

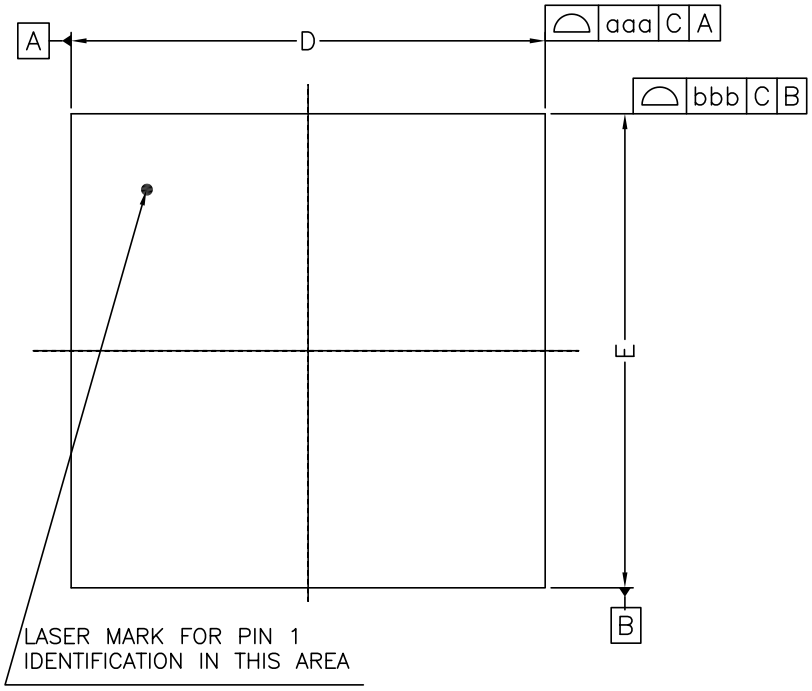
I2C frame and data transfer format-

This IC supports a 7-bit I2C address (slave address = 0b101.0001). The format is MSB-bit leading. This format uses only one byte for the 8-bit RAM/REG address. When read/write in burst mode (i.e. more than one data byte in an I2C frame), the RAM/REG address will be increased by one automatically for each data byte.

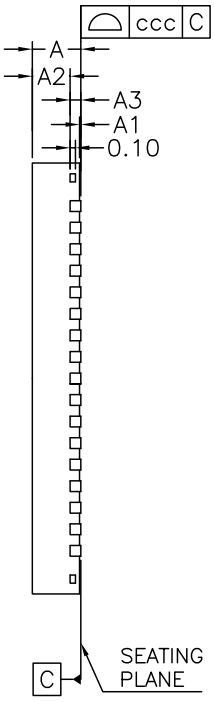
Multi-Byte Register Operation-

This IC has many registers. Some of these registers are a single byte and some are a multi-byte format. A Register's address is in unit of byte. For each multi-byte register, it forms in LSB (least significant byte) first order. The LSB byte shall have a lower address. When read/write to a multi-byte register, you must always access in the order from LSB byte to MSB byte. You should not interrupt a multi-byte register read/write with other bus operations. The writing to a multi-byte register will take effect when you are writing its MSB byte.

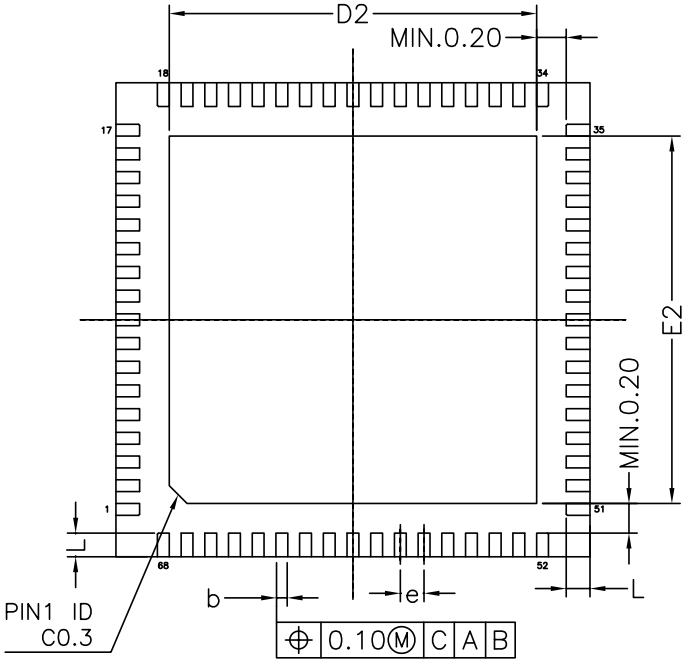
Mechanical Drawings



TOP VIEW



SIDE VIEW



BOTTOM VIEW

* CONTROLLING DIMENSION : MM

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	0.035	0.05	0.00	0.001	0.002
A2	---	0.65	0.67	---	0.026	0.026
A3	0.203 REF.			0.008 REF.		
b	0.15	0.20	0.25	0.006	0.008	0.010
D	7.90	8.00	8.05	0.311	0.315	0.317
D2	6.10	6.20	6.30	0.240	0.244	0.248
E	7.90	8.00	8.05	0.311	0.315	0.317
E2	6.10	6.20	6.30	0.240	0.244	0.248
L	0.35	0.40	0.45	0.014	0.016	0.018
e	0.40 bsc			0.016 bsc		
TOLERANCES OF FORM AND POSITION						
aaa	0.10			0.004		
bbb	0.10			0.004		
ccc	0.05			0.002		

Diagram 3: Package Dimensions

NF2004 Multi Output Clock Generator IC

CONNOR WINFIELD

Revision History

Revision	Revision Date	Note
00	09/20/17	Initial Release
01	03/25/19	Updated New Drawings - Block Diagram, Mechanical and Pins
02	09/12/19	Updated Pin #67 and Functional Diagram
03	07/16/20	Updated Notes on Pin Descriptions
04	01/12/21	Updated Pin Descriptions