P R O D U C T   B R I E F

NS2000-1PPS – Complete Sync Timing System ASIC for Synchronous Ethernet / IEEE1588 Systems

CONNOR WINFIELD

Overview

The NS2000-1PPS is a highly integrated time and frequency synchronizing ASIC. This design implementation is dedicated for use in applications which specifically require locking to an incoming 1PPS reference signal. This high precision phase and frequency synchronization solution also integrates low noise frequency generation and/or frequency translation. This product can be used to support a high-stability frequency reference for use in wireless systems, IEEE 1588v2, and applications employing a 1PPS frequency source for high precision, long term time and frequency generation.

The NS2000-1PPS allows the user access to the chip's internal phase detector to calibrate and correct for saw tooth error typically found on a 1PPS signal emanating from a GNSS receiver. Another feature provides the user access to the internal master clock and NCO which can be used to calibrate and correct for drift found in the external supporting OCXO or TCXO. With less than 1 ppt resolution, the user may compensate in holdover mode for frequency instabilities due to temperature change or long term aging characteristics.

An external precision OCXO or TCXO provides the system's master clock for various holdover performance options as well as the support for multiple filter bandwidth options from <1mHz to .05 Hz. Up to two external disciplined VCXOs provide the output characteristics for phase noise and jitter performance for any combination of 10 differential or 21 single ended clock outputs with output jitter performance options of sub100fs RMS (12kHz to 20MHz).
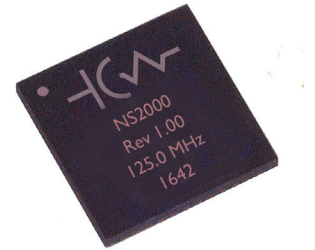
Features

- Accepts 1 PPS Reference input
- Programmable phase alignment of outputs to 1 PPS reference input
- Internal NCO for SAW tooth error smoothing
- Locked, HO, & Free-run indication. Holdover options available to .001ppb resolution
- 1Hz to 800 MHz clock output frequency range
- Ten differential or up to 23 single ended Low Jitter Clock Outputs
- Programmable output transmitters (programmable as either 1 LVPECL, 1 LVDS or 2x LVCMOS output)
- Low jitter clock outputs (less than .3ps RMS (12kHz to 20MHz) with options for sub 100fs)
- Programmable bandwidth settings for multiple applications
- I2C Interface for system communication and interrogation.
- 3.3VDC Supply Voltage
- -40C to +85C operating temperature range
- 10 x10 mm 88 pin QFN surface mount package

Applications

- Primary Reference Time Clock (PRTC) [G.8272]
- Telecom Grand Master [G.8273.1]
- Telecom boundary clock [G.8273.2]
- Wireless Base Stations
- GNSS Disciplined Oscillator
- NTP Stratum 0 Standard

NS2000-1PPS Functional Block Diagram
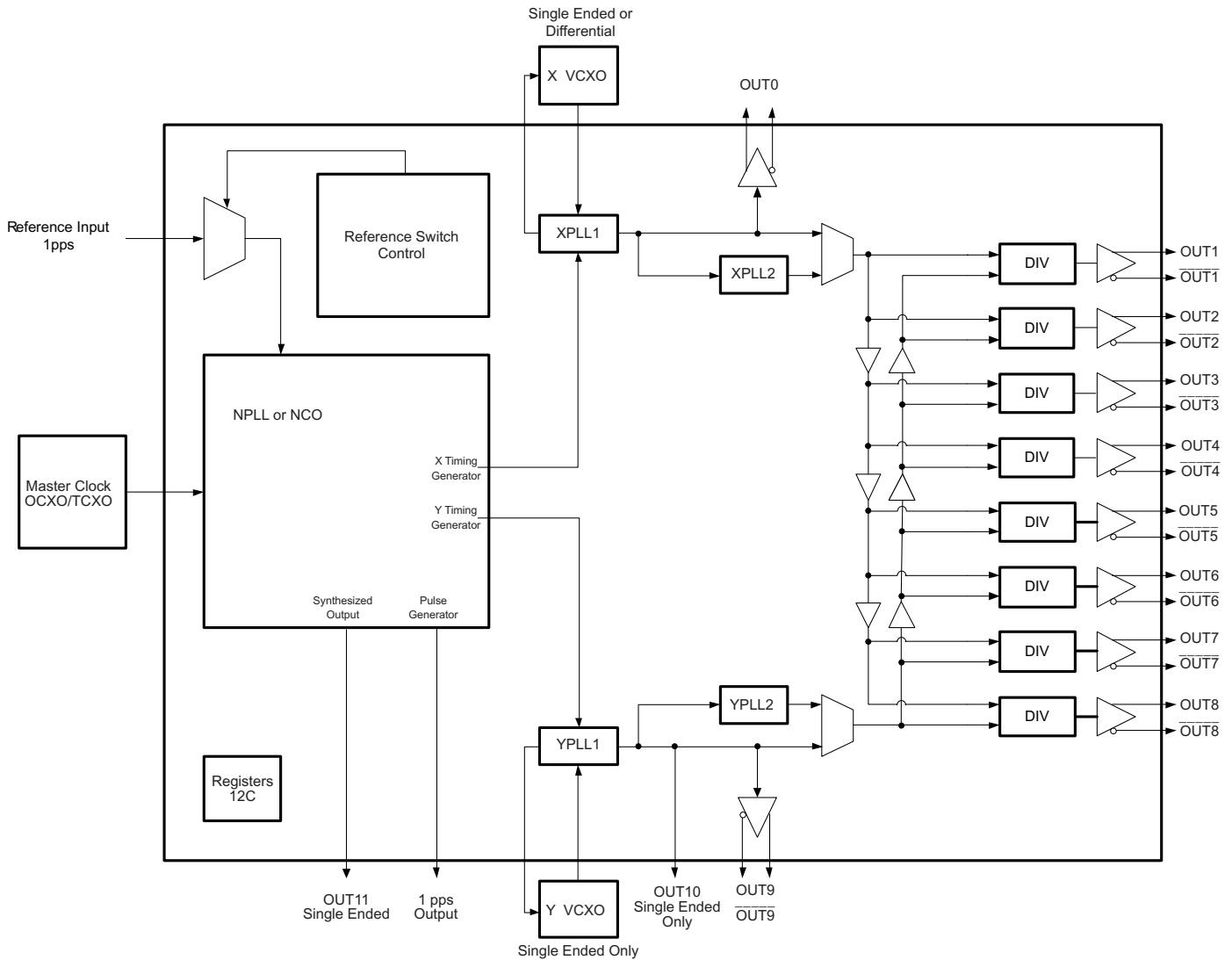
NS2000-1PPS Specifications

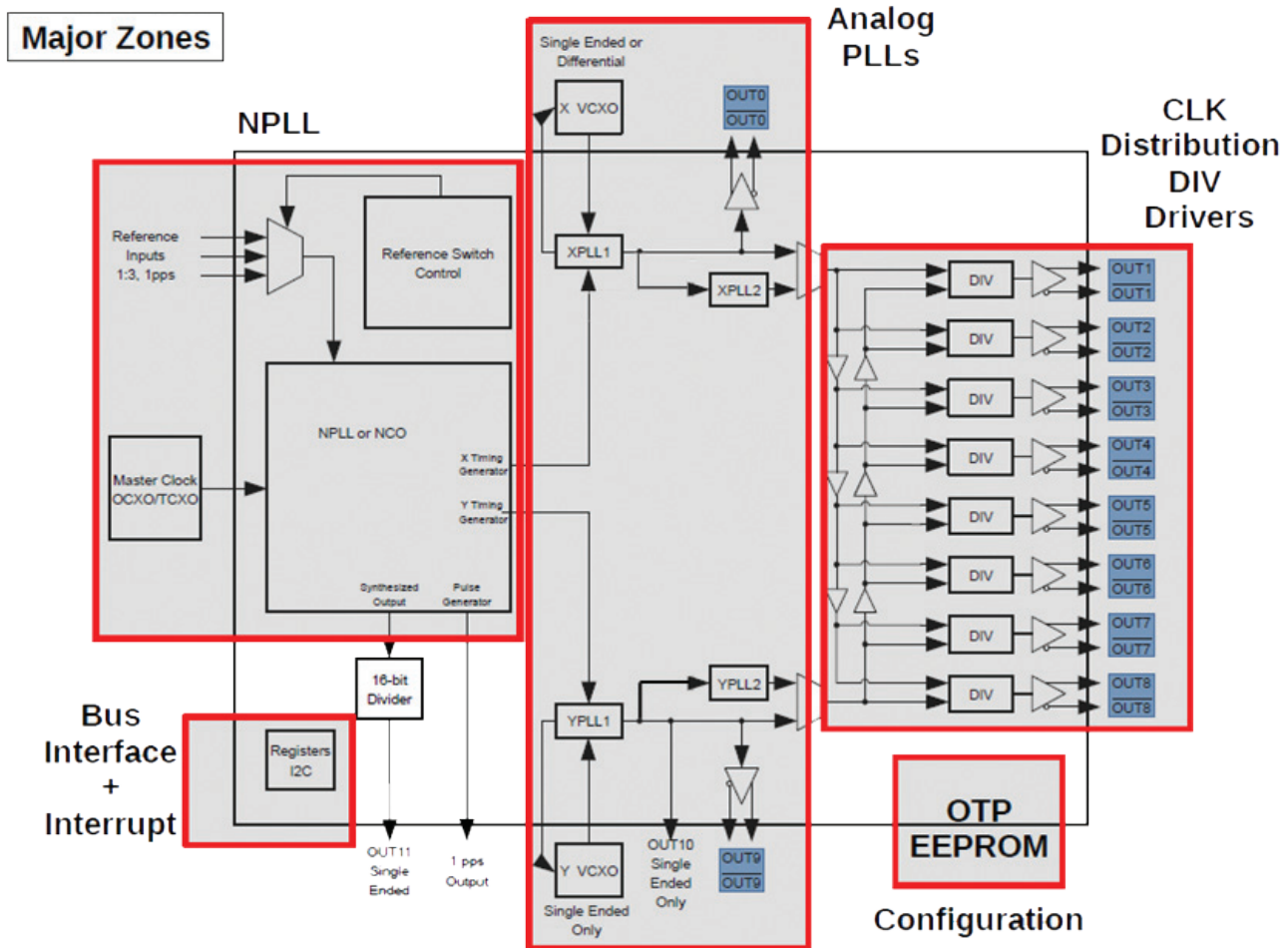| Parameter	Specification
Voltage	3.3V ±5%
Power	Based on configuration (300mA with outputs tri-stated)
	Outputs add: LVPECL 50mA, LVDS 20mA, LVCMOS 8mA
Temperature	-40 to 85°C Industrial temp range operation
Reference Frequency (1PPS)	1 Pulse Per Second (1Hz) 3.3 V DC ref
Low Jitter Clock Output Frequency	1Hz to 800 MHz
DPLL Synthesized Output Frequency	10MHz to 80MHz plus 1 PPS
Holdover stability	0.001 ppb capable
Dimensions	10 x 10 x 1mm 88 pin QFN package

General Description

The NS2000-1PPS is a highly integrated PLL time and frequency synchronizing integrated circuit that receives a single 1PPS reference input and generates multiple outputs locked to the rising edge of the 1PPS pulse. The 1PPS reference can be generated from a GNSS source. The chip is capable of correcting for the 1PPS signal's quantization error effectively reducing the saw tooth error typically found on GNSS receiver generated 1PPS signals.

The design architecture incorporates a sophisticated digital and analog PLL scheme to provide up to 23 phase/frequency locked clock outputs at frequencies from 1.5 kHz to 800 MHz including a 1PPS pulse generator output. The system is clocked with an external precision OCXO or TCXO providing the basis for various holdover and free run performance options. A variable bandwidth filter (0.35 mHz to .05 Hz) enables supporting phase locking to high jitter 1 PPS input references to less than 1ns resolution. The phase relationship between the 1PPS input reference and output ports can be controlled with programmable settings.

The chip digitally synthesizes up to four independent frequencies from the timing generator. Two outputs are brought out directly from the NPLL synthesizer (including the 1PPS pulse generator) and another two outputs function as reference inputs to the two analog PLL chains within the chip. These two signals can be attenuated internally to ultra low jitter levels and provide the source for multiple output clocks in the chip's clock distribution section.

The analog portion of the chip consists of two independent PLL chains (X side and Y side) that attenuate jitter through a variety of optional configurations to achieve the user's desired performance level. The chip can operate with either X side or Y side analog PLLs or outputs can be generated from a combination of both X and Y side. One or two disciplined VCXO(s) provides the output characteristics for phase noise and jitter performance for up to 21 clock outputs (10 differential or 21 single ended) with optional configurations that can provide output jitter performance of less than 100fs RMS over the integration range of 12 kHz to 20MHz. The 1 PPS pulse generator is independently controlled and a 1PPS pulse can be generated in holdover mode.

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Internal NPLL and Numeric Timing Generator

The kernel of the NS2000-1PPS is a digital-based numerical PLL. In its core, all internal modules are either digital or numerical, including the phase detectors, filters, timing generator and clock synthesizers. The pure digital design timing generator allows the NS2000-1PPS to become an accurate and reliable deterministic system.

The NS2000-1PPS includes a single timing generator. This timing generator can individually operate in free run, synchronized, and holdover mode. The timing generator must be placed in either external-timing mode or self-timing mode via register settings. External timing mode supports "synchronized" mode. In external timing mode, the systems NPLL phase locks to the 1 PPS external reference input. In "synchronized" mode, the NS2000-1PPS's PLL loop bandwidth may be programmed from <1mHz to .05 Hz to vary the timing generator's filtering function.

Self-timing mode supports "free run" and "holdover" modes. In self-timing mode, the PLL simply tunes the clock synthesizers to a given fractional frequency offset. When the 1PPS reference input and previous holdover history are unavailable, such as in system's initialization stage, free-run mode will be entered and used. When the selected reference input is unavailable but a long-term holdover history accumulated in previous synchronized mode is available, holdover mode may be entered or used. In NS2000-1PPS, the free-run clock is derived from the MCLK (external oscillator) and digitally calibrated to compensate the external oscillator's accuracy offset.

Four internal clock synthesizers generate output signals at any frequency (divisible by 8 kHz) from the systems timing generator. Two of these outputs are used internally as reference inputs to the X and Y side analog PLL chain. The output frequency of the synthesizers which support the X and Y side analog PLL chains are register programmable to any frequency divisible by 8 kHz.(8 kHz * M where 1 < M <=5000). A third generates a 1PPS pulse and the fourth is brought out directly to the user (output 11) as a singled ended CMOS 3.3V signal. Output 11 has a frequency range from 10Mhz to 80MHz and is register programmable. The synthesized clocks are phase and frequency locked to the internal NPLL.

The system timing generator is supported by an internal numerically controlled oscillator (NCO) that is timed by the systems master clock. The NS2000-1PPS reports to the user the frequency offset between that of the system master clock and that of the incoming reference in "Locked" mode. When in "holdover" mode, the NCO's frequency offset can be externally controlled via registers in the chip to calibrate the master clock. This functionality allows the user to externally compensate the NCO output to address drift from temperature fluctuations and/or long term drift characteristics of the external OCXO or TCXO. The NCO offset control has a resolution of less than 1 part per trillion.

Master Clock (MCLK) and Programmable Bandwidth Settings

The system's master clock (MCLK) requires a "fixed" frequency clock input and is used to clock the NS2000-1PPS NPLL. The NS2000-1PPS can be configured to accommodate one of four master clock frequencies, 10MHz, 19.2 MHz, 20 MHz or 24.576MHz, via state settings on pins 47 and 63.

The master clock's performance characteristics should be consistent with chosen bandwidth settings and desired holdover and free run performance requirements. Bandwidth setting options are programmable in the NS2000-1PPS from .35 mHz to approximately .05 Hz. When locking to a high jitter 1PPS input signal, a low bandwidth filtering algorithm should be employed using a bandwidth setting in the NS2000-1PPS below 1mHz. For optimal performance when using low bandwidth settings, the short term stability level of the master clock should be consistent with the Stratum 3E performance requirement. Using a bandwidth setting of .35 mHz and an appropriate master clock, the 20ns jitter from a typical 1PPS GNSS source can be reduced into the range of <1ns. Higher bandwidth settings like .05Hz, can be supported by a TCXO with the appropriate short term stability specification. A variety of master clock options are available from Connor-Winfield to support the NS2000-1PPS .

The desired frequency input choice is hardware controlled and can be configured by setting the appropriate pins (Pin 63 and Pin 47) to the specific logic level as shown in the table below.

MCLK Frequency Desired	Pin 63 MCLK_Rate 1	Pin 47 MCLK_Rate 0
10.0 MHz	0	0
20.0 MHz	0	1
19.20 MHz	1	0
24.576 MHz	1	1

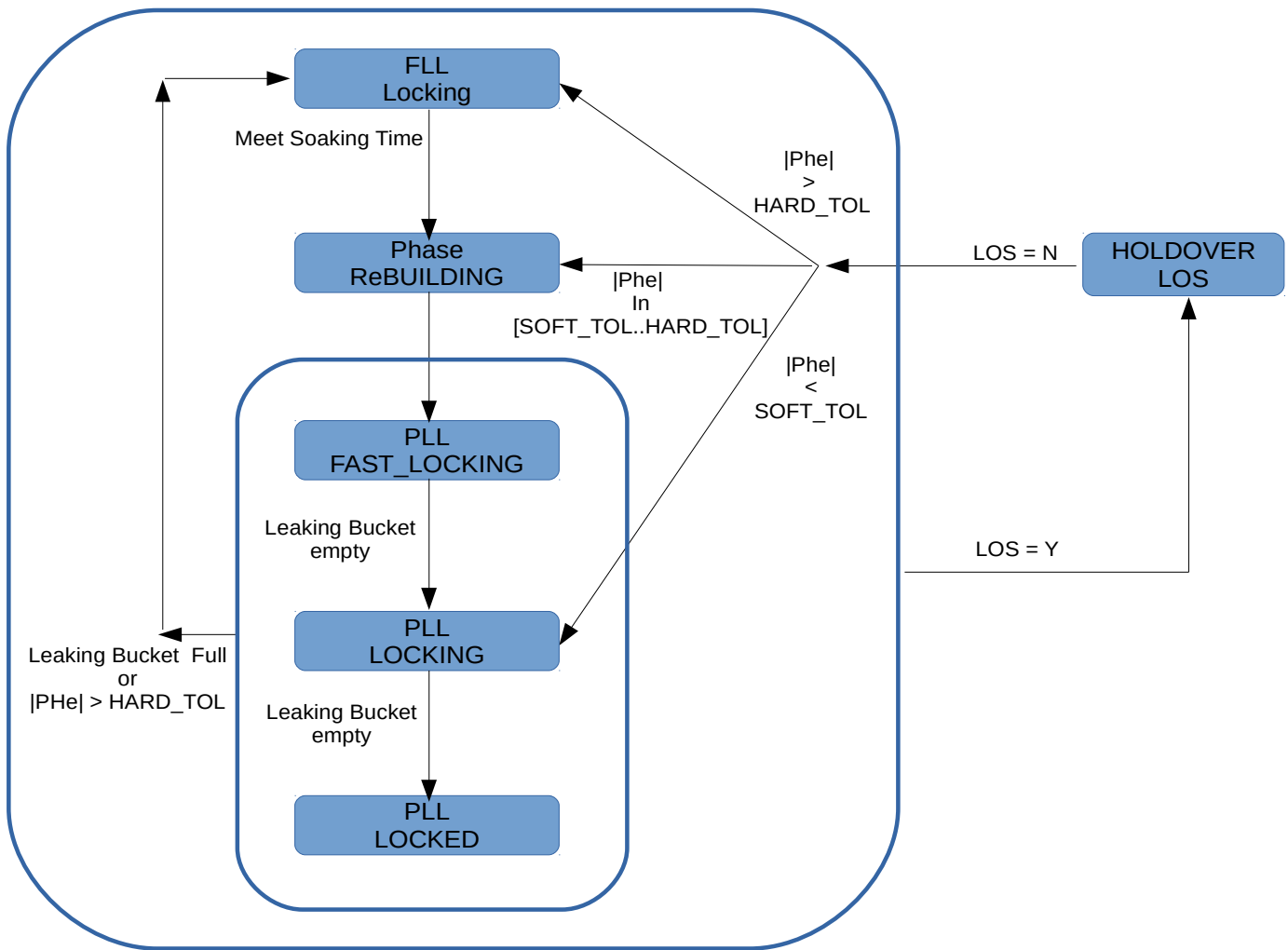Table 1 Master Clock Frequency Selection list

Phase Synchronization General

The NS2000-1PPS reports through its registers the raw phase error between the 1PPS output and the 1PPS input and the fractional frequency offset of the system's master clock as compared to the incoming reference input. It also reports the status of the NPLL when phase locking to a valid 1PPS incoming reference signal. The NS2000-1PPS digital core generates essentially four synchronized clocks. Two of the four synthesized outputs become the frequency input source for the two internal analog PLL chains (X and Y). These two synthesized clock outputs can be programmed to any frequency divisible by 8 kHz to support phase / frequency matching in the downstream analog clean up APLL portion of the IC. In synchronized mode, the phase relationship between the selected reference input and the clock output may be phase arbitrary or frame phase aligned. A zero frame phase relationship is produced by programming in frame phase align mode. The additional two synthesized and phase aligned outputs includes a 1 PPS pulse generator and a "flexible" frequency single ended output synthesized from the NPLL (output 11). Output 11 has a programmable frequency range of 10MHz to 80MHz in multiples of 8 kHz and is register programmable.

The phase skew between the X and Y side of the chip can be programmed to a zero level aligned to the reference inputs. There is a fixed skew delay through the output banks of the chip as described below in the Output Transmitter Ports section.

1PPS Locking and Phase Synchronization Solution

The NS2000-1PPS phase locking design implementation employs a low bandwidth filtering scheme with multiple locking stages during the complete phase locking process.

All configuration register settings (all registers for PLL1/PLL2/OUT and all registers for the NPLL's parameters) must be initialized upon start up of the NS2000-1PPS. After power on, the system initially enters a "Free Run" mode, with the NPLL turned off. The master clock will synthesize a clock to send to X and Y PLL chains at the MCLK's free running accuracy. It will not, however, generate a 1PPS output in the initial Free Run state. When the user writes '1' to register (NPLL_START), the NPLL will start to operate. At this moment, the NPLL will ignore any change attempted in those configuration registers, reacting only to three run-time registers: reg(NPLL_MANUAL_CTRL), reg(NPLL_PD_CALI), and reg(NPLL_MCLK_CALI).

From its initial Free Run state and once reg NPLL_START is set to "1", the NPLL will look for the existence of a 1PPS input signal. If a reference input signal exists, the NS2000-1PPS begins the locking process with a "frequency locking" mode (FLL_LOCKING). In the first stage of the locking process, the frequency is disciplined before the phase build out process can begin. The FLL low-pass filter band is register settable from 179mHz to 22mHz. The user defines the frequency offset (in ppb) the system can tolerate to be considered frequency "locked" (frequency difference tolerance). A "soak time" is defined through register settings for the frequency locking process. The soak time (in seconds) establishes the minimum amount of time the system's NPLL must stay within the frequency-locked tolerance before the system can move on to the phase locking operation.

ADDR	BITS	NAME	I/O	DEFAULT	DESCRIPTION
0x37	[7:0]	NPLL_FLL_PARA	R/W	0	NPLL FLL_LOCKING mode parameters
					bit[1:0] low-pass filter's band index
					(0) 179 mHz
					(1) 90 mHz
					(2) 45 mH
					(3) 22 mHz
					bit[7:2] frequency difference tolerance.(in ppb).
0x38~0x39	[14:0]	NPLL_FLL_SOAKTIME	R/W	0	NPLL FLL_LOCKING mode soaking time. 15-bit. Unit in second.
					bit[14:0] soaking time, unit(second)
					bit[15] ~ RSVD ~

Once in frequency lock, a phase error build out process begins. The NS2000-1PPS allows the user to control the speed at which the phase error build out will occur. In the PHASE REBUILDING stage, the 1 PPS output will first execute a phase jump to the location closest to the 1PPS input. Next, a phase error build out will be executed on the phase detector to eliminate the initial phase error reading. The phase error build out will be reimbursed back according to the phase shift speed chosen in the register.

ADDR	BITS	NAME	I/O	DEFAULT	DESCRIPTION
0x4C	[7:0]	NPLL_PHASE_SHIFT_SPEED	R/W	0	Phase reimbursement speed of alignment PBO (ph build-out) after PHASE ReBUILD. 8-bit. Unit in (10 ps/S)

When the phase build out process is complete, the phase locking process begins with a "Fast locking" stage. In Fast Lock stage, the chip allows the user to define a higher bandwidth setting than the final bandwidth setting chosen in "PLL Locking" and "PLL Locked" stages. In each of these three stages, a "leaking bucket" counter has been provided to allow the use to monitor the qualification status at each locking stage. The leaking bucket threshold tolerance (in ns) and size is register settable with 15 bits available.   In each locking stage, each arriving 1PPS signal is evaluated and the phase error between the 1PPS input and 1PPS output is compared and measured against the threshold level defined in the register for that particular bucket. The bucket level initially has a value of 50% of the size set in the register. The initial value of the bucket is increased by one (1) each time the phase error is out of the +/- phase error threshold level defined in the corresponding register for that bucket. The bucket value is decreased by one (1) for each pulse where the phase error falls within the +/- phase error threshold limit for that particular bucket. At each stage, if the value of the bucket reaches the bucket size limit, the system will report the bucket as being FULL/FAILED. When the value of the bucket reaches zero, the system will report the bucket as being EMPTY/PASSED, at which time the system will proceed to the next locking stage or PLL_LOCKED status.

ADDR	BITS	NAME	I/O	DEFAULT	DESCRIPTION
0x3B~0x3C	[14:0]	NPLL_LEAKBUCK_THRESHOLD	R/W	0	NPLL PLL's leaking bucket threshold. Unit(nS).
					bit[14:0] phase error threshold. unit(nS)
					bit[15] ~ RSVD ~
0x3D~0x3E	[14:0]	NPLL_LEAKBUCK_SIZE_FAST	R/W	0	NPLL PLL'S leaking bucket size in PLL_FAST_LOCKING mode
					bit[14:0] bucket size
					0bit[15] ~ RSVD ~
0x3F~0x40	[14:0]	NPLL_LEAKBUCK_SIZE_NORMAL	R/W	0	NPLL PLL's leaking bucket size in PLL_LOCKING and PLL_LOCKED mode
					bit[14:0] bucket size
					bit[15] ~ RSVD ~

Holdover and Loss of Signal (LOS)

Holdover mode is available after the system has successfully locked to a valid 1PPS reference input signal. There are two ways in which the system can move into holdover mode. Register 0x36 [7:0] NPLL_MANUAL_CTRL allows the user to manually force the system into a Loss of Signal (LOS) mode. The other is when the system detects that no signal exists on the incoming reference. This condition will put the system into Holdover mode. Through its internal counter, the NS2000-1PPS can detect the existence of a 1PPS signal, however, it does not perform any qualification evaluation of the validity of the 1PPS signal.

In return from Holdover mode, the NS2000-1PPS design allows the user to set phase error tolerance threshold levels to control the sequence when re-entering the locking process. Settings for Soft Tolerance (NPLL_PHe_SOFT_TOLERANCE) and Hard Tolerance (PHe_HARD_TOLERANCE) are available which are effectively used to reduce the potential locking time depending upon the conditions during holdover mode.

When recovering from loss of signal and reentering from holdover, if the absolute phase error is less than the soft tolerance threshold (NPLL_PHe_SOFT_TOLERANCE) set in the register, the system will move directly to the PLL_LOCKING mode, effectively bypassing the frequency locking (FLL_LOCKING) mode and

PHASE REBUILDING modes. If the absolute phase error falls between the Soft and Hard tolerance threshold limits, the system will move directly to the Phase Build stage. If the absolute phase error exceeds the Hard tolerance (PHe_HARD_TOLERANCE) threshold, the system will return to the Frequency locking stage (FLL_LOCKING) and proceed through the complete locking stages of operation. The PHe_HARD_TOLERANCE threshold level is used as the phase error tolerance limit in any PLL mode and once the phase error violates the Hard tolerance threshold level, the NPLL state-machine will be switched to the FLL_LOCKING mode.

ADDR	BITS	NAME	I/O	DEFAULT	DESCRIPTION	
0x36	[7:0]	NPLL_MANUAL_CTRL	R/W	0	NPLL's manual control	
					bit[0]:	1: manually forced LOS; 0: normal
					bit[7~1]	~ RSVD ~
0x41~0x42	[14:0]	NPLL_PHe_SOFT_TOLERANCE	R/W	0	NPLL's soft phase error tolerance. Unit in nS.	
					bit[14:0]	soft tolerance, unit(nS)
					bit[15]	~ RSVD
0x43~0x44	[14:0]	NPLL_PHe_HARD_TOLERANCE	R/W	0	NPLL's hard phase error tolerance. Unit in nS.	
					bit[14:0]	hard tolerance, unit(nS)
					bit[15]	~ RSVD ~

Phase Detector Calibration/Saw Tooth Error Correction

The NS2000-1PPS provides access to the chip's internal phase detector to enable an adjustment to address and correct for the Saw tooth noise inherent in most 1PPS signals generated from a GNSS receiver. The register has a range of -32,768 to +32,767 to calibrate the numerical phase detector's offset being reported by the system. The register value must be ready when its associated 1PPS input pulse arrives. The readiness of this register's value must be compliant to a minimum set time (10uS) and hold time (125 uS). Generally, quantization error reported by the GNSS receiver is used to support this register's functionality.

ADDR	BITS	NAME	I/O	DEFAULT	DESCRIPTION
0x4D~0x4E	[15:0]	NPLL_PD_CALI	R/W	0	NPLL phase detector offset calibration. 16-bit 2's complement.
				Unit in pS.	

Frequency Offset Calibration

The NS2000-1PPS provides the user an ability to digitally fine tune its internal master clock. . The calibration range is ~ +/- 114 ppm. The internal master clock is boosted in frequency from the external clock source used. In holdover mode, this feature can be used to accommodate for predictable drift in the external clock to compensate for changes in frequency due to temperature change or long term drift due to aging. Using an OCXO that has been designed for temperature coefficient correction can be used in conjunction with this feature. This feature provides the user a resolution of < 1 ppt per step. Negative values decreases the frequency. Positive values increases the frequency.

ADDR	BITS	NAME	I/O	DEFAULT	DESCRIPTION	
0x4F~0x54	[47:0]	NPLL_MCLK_CALI	R/W	0	NPLL MCLK's fractional frequency offset calibration. 28-bit 2's complement. Unit in (0.851495 ppt)	
					bit [27:0]	calibration offset, 2's complement unit (0.851495 ppt)
					bit [47:28]	~ RSVD ~

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EVENT_INTR

The NS2000-1PPS provides an event interrupt notification function (EVENT_ INTR pin 4). This pin's sole function is to notify the user when the NPLL_MODE status changes.

In this one bit register, the interrupt pin becomes "active" when at least one bit is non-zero. The current interrupt status can be read from this register. Once the interrupt pin is activated, it can only be deactivated when the interrupt status has been erased. The user can write to this register, however, its operation is not "write-the-value- then–replace-the-value". It is a bit-operation. For each bit, write "1" to erase that bit value. It can be stated as: INTR_STATUS = INTR_STATUS & (~VALUE).

ADDR	BITS	NAME	I/O	DEFAULT	DESCRIPTION	
0x07~0x08	[15:0]	INTR_EVENT	RW	0	Interrupt Event	
					bit[0]	REG(NPLL_MODE) value changed
					bit[15~1]	~ RSVD ~
0x09~0x1F		~ RSVD ~				
0x20	[2:0]	NPLL_MODE	R		NPLL_MODE	
					0:	HOLDOVER_LOS
					1:	FLL_LOCKING
					2:	PHASE_ReBUILDING
					3:	PLL_FAST_LOCKING
					4:	PLL_LOCKING
					5:	PLL_LOCKED
					6,7:	~ RSVD ~

1PPS Output

The 1PPS output's pulse width can be programmed in the NS2000-1PPS.

ADDR	BITS	NAME	I/O	DEFAULT	DESCRIPTION
0xA0~0xA1	[11:0]	1PPS_PULSE_WIDTH	RW	10	1PPS output pulse width. Unit in uS.

Phase Alignment to Clock Outputs

The NS2000-1PPS can be configured to phase align the 1PPS output with frequencies outputs generated in the two analog PLL chains driven by the synthesized outputs from the NPLL's timing generator. Both X and Y side APLL chains can be set to align with the 1PPS output (NPLL_ALIGNED_PATH). If both PLL X and Y are programmed to be aligned to the 1PPS output and assuming different clock frequencies are used for the VCXOs supporting the X and Y side, it is recommended, if possible, to use a common divided down clock frequency for each respective supporting synthesizer output from the NPLL. However, the higher the frequency specified as the common divider frequency, the smaller the phase error that will need to be built out in the phase rebuilding stage.

ADDR	BITS	NAME	I/O	DEFAULT	DESCRIPTION	
0x45	[1:0]	NPLL_ALIGNED_PATH	R/W	0	Clock path selection to phase aligned to 1PPS output.	
					bit[0]:	XPLL: 1:YES, 0:NO
					bit[1]:	YPLL: 1:YES, 0:NO
					bit[2, 3]: DNC	
					bit[7~2]:	~ RSVD ~
0x46~4B	[47:0]	NPLL_ALIGNED_OUT_FREQ	R/W	0	The output frequency of the aligned clock path. 17-bit. Unit in 8kHz.	
					bit [16:0] n, freq = 8kHz x n	
					bit [47:17] ~ RSVD ~	

NS2000-1PPS Analog PLL Chain General Description

The NS2000-1PPS supports two independent analog PLL chains (X,Y) to support two simultaneous, independent frequency domains that share ten programmable clock output transmitter ports. There is an additional single ended output on the Y-side (Output 10). The NS2000-1PPS consists of two (2) independent sets of two (2) cascaded PLL stages, referred to as the X and the Y side. In each X and Y side of the chip, the first stage PLL (XPLL1 and YPLL1) attenuates the initial jitter from the reference input/NPLL with the use of an external VCXO.

When in operation, the locked VCXO signal can be sent directly to the output transmitter ports for a direct pass through of the VCXO frequency or further divided using the independent 20 bit divider circuits at each output transmitter port.

Alternatively, the VCXO frequency/signal can be sent to a second stage PLL. A second stage PLL for each X and Y side (XPLL2 and YPLL2) with an integrated high frequency VCO is available to accept the output of the first stage PLL1. Each PLL2 has an integrated phase frequency detector, charge pump and VCO in the usable range of 1.2GHz to 1.475 GHz that can be employed to generate locked output clocks at the eight output transmitter ports using the eight independent 20 bit divider circuits found at each transmitter ports.

This design architecture gives the user a great deal of control over the output phase noise and jitter level generated by the NS2000-1PPS . An external VCXO with exceptional phase noise and jitter performance can be used in bypass mode of the NS2000-1PPS to retain the ultra-low jitter performance characteristics with very little additive jitter contributed by the NS2000-1PPS . Low frequency VCXO sources (as low as 1 MHz) as well as differential clock sources (up to 800 MHz) can be used in bypass mode to achieve maximum jitter attenuation. If outputs are generated using PLL2, single ended VCXOs at frequencies between 40 MHz and 100 MHz should be used for best performance. Depending upon the external VCXO configuration used, clock outputs can be generated in the frequency range from 1Hz to 800MHz, limited to 180MHz for LVCMOS outputs.

PLL1 (X,Y) General Description

PLL1's (X,Y) function in the NS2000-1PPS it to act as a frequency translator and jitter attenuator. PLL1(X,Y) effectively attenuates the jitter from the incoming reference clock and translates the frequency to that of the chosen external VCXO which supports it. PLL1(X,Y) can pass through the external VCXO frequency directly to the output dividers and transmitters or be used as the input frequency to the second stage PLL, PLL2 (X,Y). When the VCXO clock output is passed directly through to the output dividers and transmitters, the NS2000-1PPS is capable of attenuating the jitter with approximately 10fs additive jitter to that of the external 3.3V VCXO.

PLL1(X,Y) consists of a phase-frequency detector (PFD), charge pump, passive loop filter, and an external VCXO operating in a closed loop. PLL1(X,Y) has the flexibility to operate with a loop bandwidth of approximately 10Hz to 200 Hz. This relatively narrow loop bandwidth gives it the ability to suppress jitter that appears on the synthesized clock signal feeding PLL1 from the NS2000-1PPS 's NPLL. This synthesized clock eliminates the requirement for a phase detector frequency relationship between the frequency of the reference inputs into the NS2000-1PPS and the output VCXO frequency desired. The NPLL's synthesizer frequencies are programmable allowing for a flexible phase detector rate however the PFD rate must be divisible by 8kHz (8 kHz * M where <1 M <=5000). The charge pump current ,feedback divider, R0,and R2 are register programmable inside the chip. Capacitors C1 and C2 are internal and are fixed values. One external capacitor is required for the NS2000-1PPS's loop filter, which connects to pins Pump_C0+ and Pump_C0- . An optional external filter on the control voltage pin of the external VCXO is supported through Buf_Out1 and Buf_Out2 pins.


PLL 1 Circuit Diagram (X , Y)
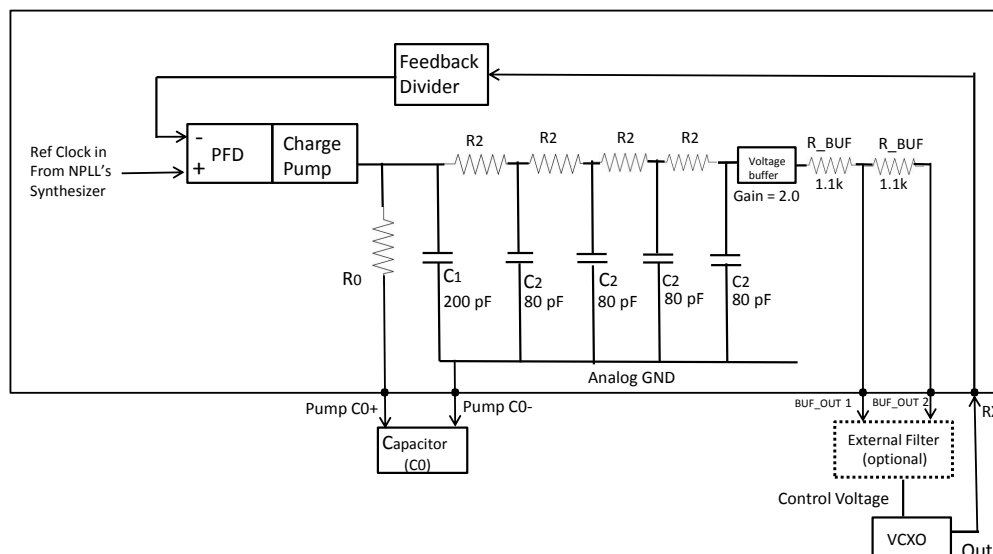
PLL2 (X, Y) General Description

PLL2(X,Y) operates as a second stage analog PLL block, taking its reference input from PLL1 (X,Y). PLL2 (X,Y) consists of a fully integrated phase-frequency detector (PFD), charge pump, integrated loop filter, and integrated internal VCO operating in a closed loop. The NS2000-1PPS 's internal VCO operates in the frequency range from 2.4GHz to 2.95GHz, however an internal pre-divider (by 2) makes the effective programmable VCO frequency range available from 1.2GHz to 1.495 GHZ. Through programmable registers, the input frequency from PLL1 (X,Y) can be integer multiplied into the VCO frequency range of PLL2 (X,Y). Once locked, the chosen VCO frequency can be integer divided using the 20 bit programmable divider circuits preceding the programmable output transmitter ports.

The charge pump current, feedback divider, R0, C0 and the Kvco of the internal VCO are register programmable inside the chip. Capacitors C1 and C2 and R1 are predefined fixed values.

PLL 2 Circuit Diagram (X , Y)
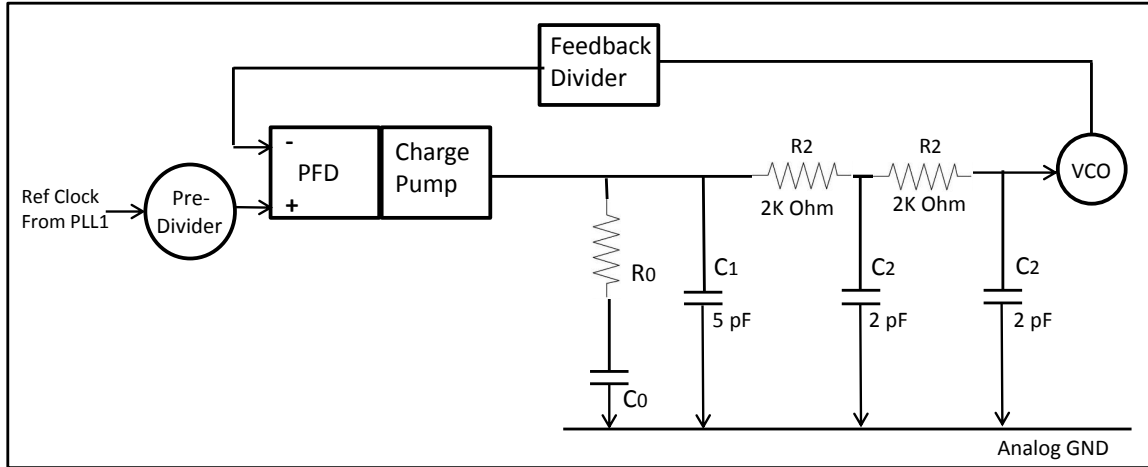
X-Side PLL Chain

On the X side of the chip, XPLL1 can be supported by a single ended or differential VCXO at frequencies from 10MHz to 800MHz.. Well-chosen high frequency VCXOs can provide jitter performance levels in the 50 to 60fs range and thus locked outputs from XPLL1 can provide well under 100fs jitter performance levels in the integration band of 12 kHz to 20MHz. This frequency can then be passed through to additional output transmitters/dividers and/or be used as an input to the second stage PLL (XPLL2) to synthesize additional output frequencies at the output transmitter ports. Outputs derived from XPLL2, depending upon frequency, will generally provide jitter performance levels of < 300fs over the integrated band of 12kHz to 20 MHz.

ADDR	BITS	NAME	I/O	DEFAULT	DESCRIPTION	
0x05	[2:0]	XPLL_Mode	RW	0	XPLL Mode	
					0,5,6,7:	Both XPLL1 and XPLL2 are power down
					1:	XPLL1 with sgl VCXO -> XPLL2
					2:	XPLL1 with diff VCXO -> XPLL2
					3:	XPLL1 with sgl VCXO; XPLL2 is power down
					4:	XPLL1 with diff VCXO; XPLL2 is power down

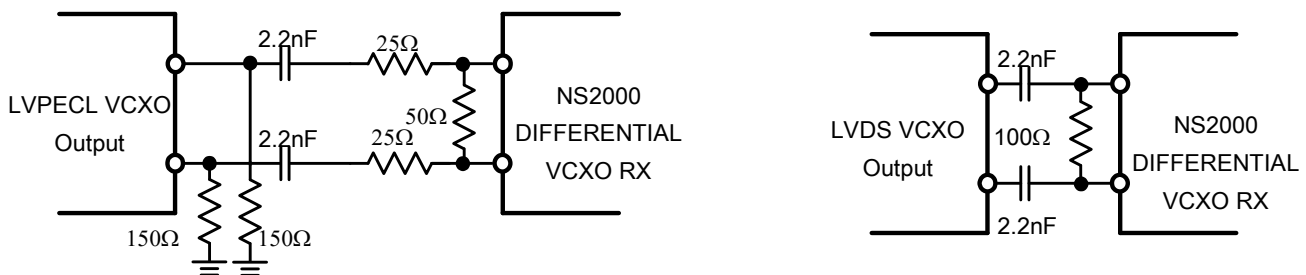### Differential VCXO termination recommendation in to pins XRX_P and XRX_N

Y-Side PLL Chain

On the Y side of the chip, YPLL1 can be supported only by a single ended VCXO at frequencies from 10MHz to 160MHz. At Output 10, the VCXO nominal frequency will bypass directly to Output 10 in order to optimize clock jitter performance with a minimal additive jitter from the chip. Output 9 is LVCMOS only which effectively acts as a buffer from the VCXO in and directly out of the chip to achieve optimal jitter (usually less than 10fs additive jitter) for ultra-low jitter applications. A well-chosen high frequency LVCMOS VCXO can provide jitter performance levels in the 60 fs range and thus locked outputs from YPLL1 can provide well under 80fs jitter performance levels in the integration band of 12kHz to 20MHz This VCXO frequency can then be passed through to additional output transmitters/dividers and/or be used as an input to the second stage PLL (YPLL2) to synthesize additional output frequencies at the output transmitter ports. Outputs derived from YPLL2, depending upon frequency, will generally provide jitter performance levels of < 300fs over the integration band of 12kHz to 20 MHz.

ADDR	BITS	NAME	I/O	DEFAULT	DESCRIPTION
0x06	[2:0]	YPLL_Mode	RW	0	YPLL Mode
					0,5,6,7: Both YPLL1 and YPLL2 are power down
					1,2: YPLL1 with sgl VCXO -> PLL2
					3,4: YPLL1 with sgl VCXO; YPLL2 is power down

Clock Distribution, Dividers and Drivers

The NS2000-1PPS generates up to 23 clock outputs on ten output transmitter ports and three single ended 3.3V clock output pins driven from various sections of the chip. Output transmitter ports 1-8 are preceded by a 20 bit divider circuits (any integer value from 1-1,048,576). The divider circuits can be used regardless whether the output were generated from PLL1 or PLL2.

Output transmitter ports 1 through 8 are driven by clocks generated from PLLs 1 or 2 on either the X or Y side of the chip. Output transmitter ports 0 and 10 serve only their respective X and Y side of the chip. The output transmitter ports consist of programmable 3-in-1 transmitters that can be configured to output either (2) LVCMOS or 1 LVDS or 1 LVPECL logic signal. Output transmitters can be powered down if not in use. When using LVCMOS mode, outputs can be generated on both output pins (P and N) of the output transmitter, or, one or the other. Polarity of the LVCMOS output at each pin is controllable.

Output 10, on the Y side of the chip, has been provided for use as a low jitter buffer that directly bypasses the Y side VCXO signal in and out of the chip resulting in the least amount of additive jitter (about 10fs). This output is intended to be used for ultra-low jitter performance requirements but will have inverted phase from the outputs that are generated through the transmitter output ports.

Output 11 is a 3.3V single ended CMOS output clock that has been provided to allow for an "any frequency" output that is synthesized directly from the NS2000-1PPS NPLL's timing generator. This output, because it is digitally synthesized, will have higher jitter than Outputs 0-10. Output 11 has a frequency range of 10MHz to 80MHz and is programmed as 8kHz * M where $1250 <= M <= 10000$.

The NS2000-1PPS also has a 1PPS pulse generator which outputs a programmable pulse width 3.3V CMOS 1PPS signal which is also derived directly from the system's timing generator.

Output Bank Details and Constant Skew Delay Description

Output transmitter ports 1 through 8 are divided into four output "banks". Each of the four output banks must be controlled as a unit. Bank0 (Output transmitters 1 and 2), Bank1 (Output transmitters 3 and 4), Bank2 (Output transmitters 5 and 6), and Bank3 (Output transmitters 7 and 8) represent four "banks" of outputs that can be controlled independently from each X and Y side of the chip. Either the X side or the Y side of the chip can access all four output banks, thus eliminating the requirement to use both sides X and Y in all applications. However, X and Y side clock signals must access output banks in order and must stop at the first output bank placed in use by the alternate side. For example, if X side uses banks 0, 1 and 2, Y side can only access bank 3 (outputs transmitters 7 and 8) or if Y side uses banks 3 and 2 (output transmitters 8,7 and 6,5), X side can only access bank 1 and 0 (outputs transmitters 1,2 and 3,4).

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Output Bank Details and Constant Skew Delay Description continued
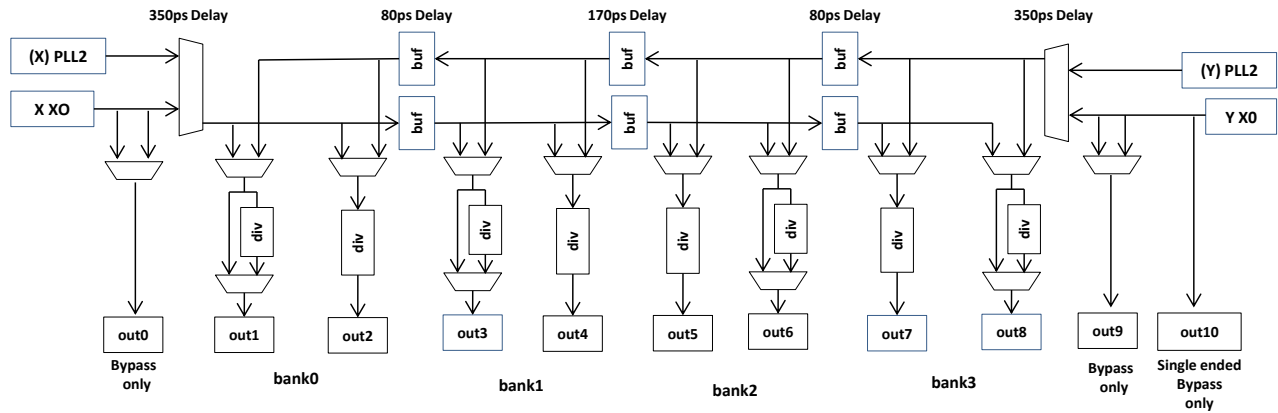
Diagram 1 Detailed Output Banks and Ports Diagram

The skew between clock outputs is constant but will exhibit a cumulative delay relative to each other based on the clock signal traveling through MUXs and Buffers. This will be dependent upon how the output banks are configured from each X and Y side. Delay times are identified in Diagram 1. The phase skew alignment of the reference inputs to the X and Y side VCXO can be programmed to a zero level using register settings.

Symmetry Control for low value odd dividers

Due to overall power limitations in the chip, only output transmitter circuits 2, 4, 5 and 7 have, by default, output symmetry control when dividing by a low, odd integer value. In circumstances which require dividing the VCO output frequency by values of 3, 5, 7 or 9, one of these output transmitter circuits should be used to achieve 50/50 duty cycle. When using an odd divider value of greater than nine (9), symmetry control is generally not required to maintain reasonable symmetry in the output. The output ports offering symmetry control do not allow for a direct by-pass through of the reference input frequency and require dividing at the output transmitter circuit by a minimum by 2. Output ports 1, 3, 6 and 8 can by-pass the divider circuit entirely or can divide by any integer number up to the 20bit value.

Output Phase Noise Characteristic Examples:

Phase noise generated from PLL2: 640MHz using 80MHz VCXO
260fs (12kHz-20MHz)
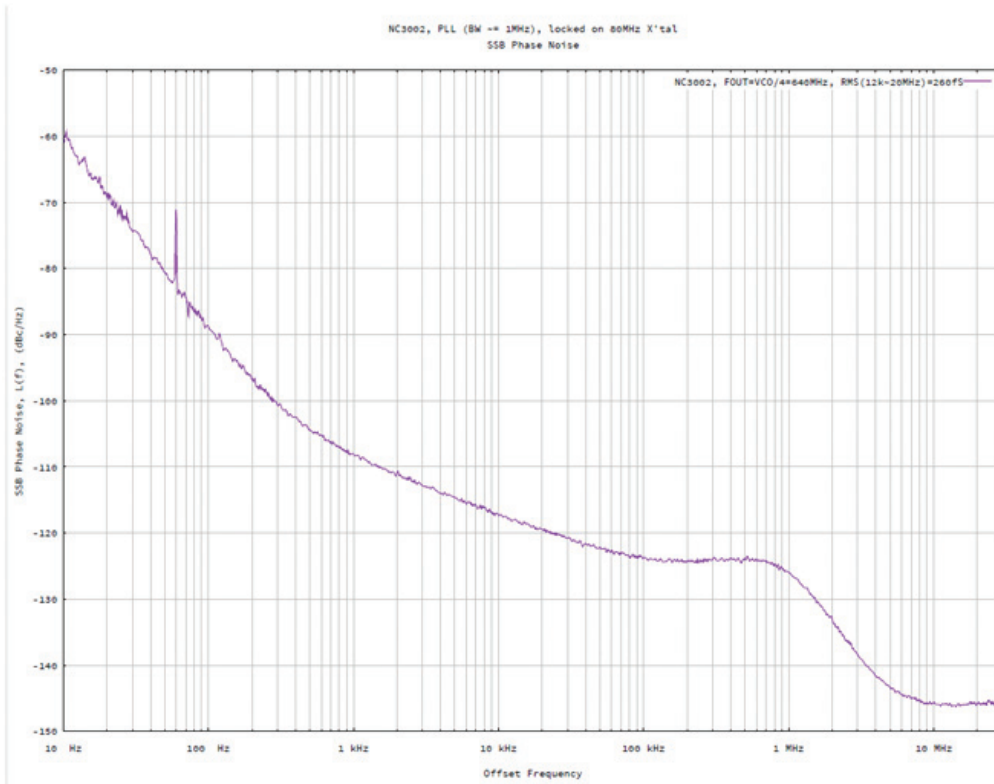
Phase noise generated from PLL1(y): 122.88MHz 63fs (12kHz-20MHz)
(using Connor Winfield model V7223T-122.88MHz LVCMOS 5x3.2mm VCXO)

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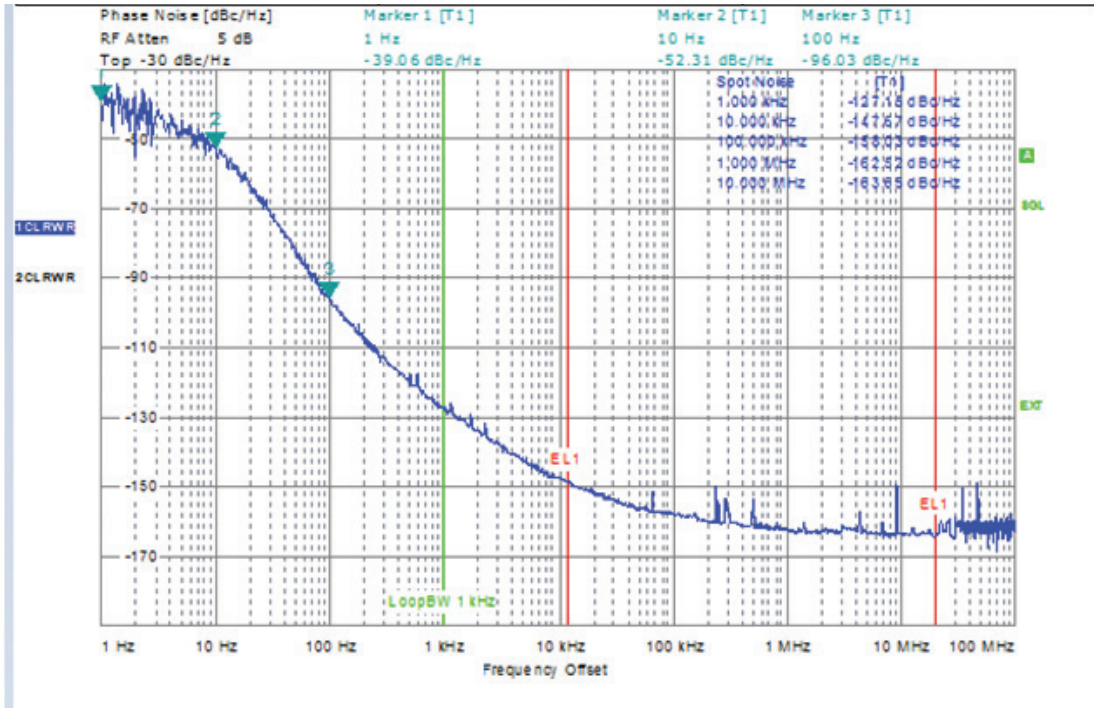
NS2000-1PPS LVPECL Suggested Termination
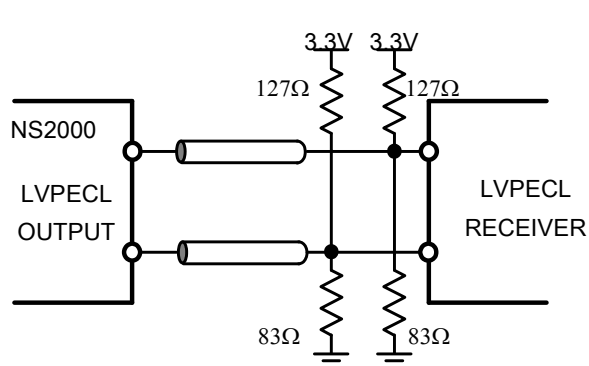
DC-Coupled LVPECL Termination
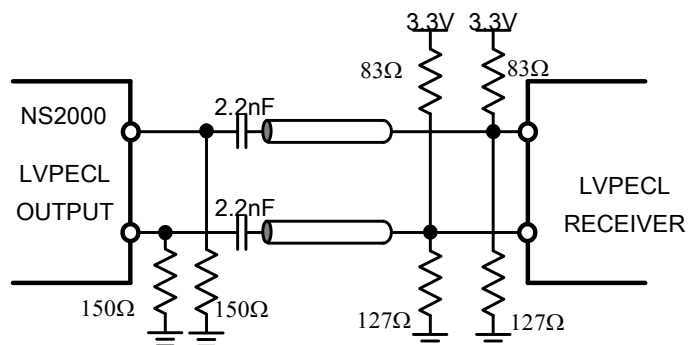
AC-Coupled LVPECL Termination

LVPECL Current Consumption
fvco=1.244GHz, fvcxo=38.88MHz,ftcxo=20MHz

OUTPUT FREQUENCY (MHz)	DUTY CYCLE (%)	RISE TIME (20%~80%)(ps)	CURRENT CONSUMPTION (mA)	DIFFERENTIAL SWING (Vp-p)
38.88	50.09	590	41.69	1.183
103.681	49.97	570	41.59	1.139
113.108	45.44	560	41.59	1.148
124.417	49.98	570	41.57	1.161
138.239	44.49	520	41.53	1.171
155.519	49.98	530	41.56	1.152
177.74	43.06	570	41.56	1.163
207.362	50.1	510	41.41	1.182
248.836	42	430	41.34	1.095
311.054	50.14	500	41.32	1.049
414.736	35.64	370	41.53	0.86
622.115	51.05	270	41.56	0.778

NS2000-1PPS LVDS Suggested Termination
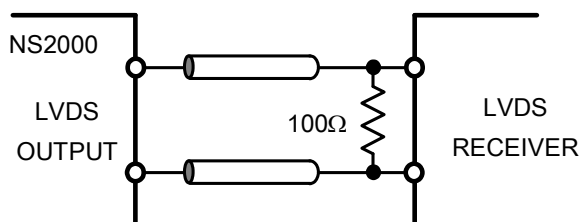
DC-Coupled LVDS Termination
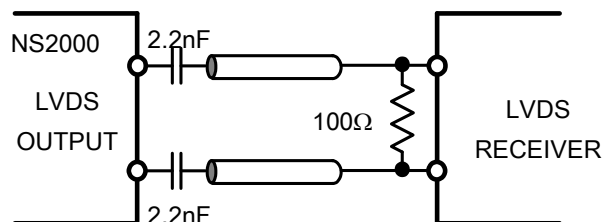
AC-Coupled LVDS Termination

LVDS Current Consumption
fvco=1.244GHz, fvcxo=38.88MHz,ftcxo=20MHz

OUTPUT FREQUENCY (MHz)	DUTY CYCLE (%)	RISE TIME (20%~80%)(ps)	CURRENT CONSUMPTION (mA)	DIFFERENTIAL SWING (Vp-p)
38.8815	49.97	700	18.18	0.593
103.68	50.18	620	18.26	0.586
113.107	50.46	600	18.26	0.593
124.414	50.21	610	18.26	0.606
138.241	50.52	580	18.26	0.61
155.52	50.26	600	18.26	0.6
177.737	50.81	610	18.26	0.598
207.363	50.52	600	18.25	0.623
248.832	50.8	450	18.25	0.575
311.05	50.62	580	18.26	0.547
414.733	49.57	250	18.27	0.431
622.108	50.9	220	18.24	0.378

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NS2000-1PPS Register Table

ADDR	BITS	NAME	I/O	DEFAULT	DESCRIPTION		
0x00~0x01	[15:0]	Chip_ID	R	0x2D00	Chip ID, it reflects the current product ID		
0x02	[7:0]	Chip_REV	R	0x02	Chip Revision		
0x03	[7:0]	Chip_Sub_REV	R	0x03	Chip Sub revision		
0x04	[7:0]	NPLL_FW_REV	R	0x04	NPLL's Firmware Revision		
0x05	[2:0]	XPLL_Mode	RW	0	XPLL Mode		
					0,5,6,7:	Both XPLL1 and XPLL2 are power down	
					1:	XPLL1 with sgl VCXO -> XPLL2	
					2:	XPLL1 with diff VCXO -> XPLL2	
					3:	XPLL1 with sgl VCXO; XPLL2 is power down	
					4:	XPLL1 with diff VCXO; XPLL2 is power down	
0x06	[2:0]	YPLL_Mode	RW	0	YPLL Mode		
					0,5,6,7:	Both YPLL1 and YPLL2 are power down	
					1,2:	YPLL1 with sgl VCXO -> PLL2	
					3,4:	YPLL1 with sgl VCXO; YPLL2 is power down	
0x07~0x08	[15:0]	INTR_EVENT	RW	0	Interrupt Event		
					bit[0]	REG(NPLL_MODE) value changed	
					bit[15~1]	~ RSVD ~	
0x09~0x1F		~ RSVD ~					
0x20	[2:0]	NPLL_MODE	R		NPLL_MODE		
					0:	HOLDOVER_LOS	
					1:	FLL_LOCKING	
					2:	PHASE_ReBUILDING	
					3:	PLL_FAST_LOCKING	
					4:	PLL_LOCKING	
					5:	PLL_LOCKED	
					6,7:	~ RSVD ~	
0x21~0x22	[15:0]	NPLL_INFO_EX	R		16-bit NPLL Extra Information. It could have different meaning in different NPLL_MODE		
					if in FLL_LOCKING mode		
					bit[14:0]	countdown of soaking time, unit(S)	
					bit[15]	== 0	
					if in PLL_FAST_LOCKING, PLL_LOCKING, or PLL_LOCKED mode.		
					bit[14:0]	leaking bucket's level	
					bit[15]	== 1	
0x23~0x28	[47:0]	PHe_RAW	R		Raw phase error between 1PPS output and 1PPS input. 48-bit 2's complement. Unit in nS.		
0x29~0X2E	[47:0]	PHe_CALI	R		Calibrated phase error between 1PPS output and 1PPS input. 48-bit 2's complement. Unit in nS.		
0x2F~0x34	[47:0]	OUT_FFO	R		Output's normalized fractional frequency offset to calibrated MCLK frequency. 48-bit 2's complement. Unit in ppt (=10-12)		
0x35	[0]	NPLL_START	R/W	0	Write 1 to this register to start NPLL. Once NPLL was started, it could be turned off only by IC reset or power cycle.		
0x36	[7:0]	NPLL_RT_CTRL	R/W	0	NPLL's run-time manual control		
					bit[0]:	forced into manual LOS/HOLDOVER	
						1: enable	
						0: disable	
					bit[1]:	to stop at PLL_FAST_LOCKING mode	
						1: enable	
						0: disable	
					bit[7:2]: ~RSVD~		
					<ps.1>		
					If set to enable to stop at PLL_FAST_LOCKING mode, NPLL will not move to PLL_LOCKING/LOCKED mode. This will force NPLL to stay using PLL_FAST_LOCKING's parameters until this feature is disabledl		

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ADDR	BITS	NAME	I/O	DEFAULT	DESCRIPTION
0x37	[7:0]	NPLL_FLL_PARA	R/W	0	NPLL FLL_LOCKING mode parameters bit[1:0] low-passed filter's band index (0) 179 mHz (1) 90 mHz (2) 45 mH (3) 22 mHz bit[7:2] frequency difference tolerance. Unit in ppb.
0x38~0x39	[14:0]	NPLL_FLL_SOAKTIME	R/W	0	NPLL FLL_LOCKING mode soaking time. 15-bit. Unit in second. bit[14:0] soaking time, unit(second) bit[15] ~ RSVD ~
0x3A	[7:0]	NPLL_PLL_PARA	R/W	0	NPLL PLL_FAST_LOCKING, PLL_LOCKING, PLL_LOCKED parameter bit[2:0] Loop bandwidth in PLL_LOCKING/LOCKED mode bit[5:3] Loop bandwidth in PLL_FAST_LOCKING mode bit[7:6] Damping factor Loop bandwidth: (0) 50 mHz (1) 25 mHz (2) 13 mHz (3) 6.3 mHz (4) 3.1 mHz (5) 1.6 mHz (6) 0.78 mHz (7) 0.39 mHz Damping factor (0) 0.7 (1) 1.4 (2) 2.0 (3) 3.5
0x3B~0x3C	[14:0]	NPLL_LEAKBUCK_THRESHOLD	R/W	0	NPLL PLL's leaking bucket threshold. Unit(nS). bit[14:0] phase error threshold. unit(nS) bit[15] ~ RSVD ~
0x3D~0x3E	[14:0]	NPLL_LEAKBUCK_SIZE_FAST	R/W	0	NPLL PLL'S leaking bucket size in PLL_FAST_LOCKING mode bit[14:0] bucket size 0bit[15] ~ RSVD ~
0x3F~0x40	[14:0]	NPLL_LEAKBUCK_SIZE_NORMAL	R/W	0	NPLL PLL's leaking bucket size in PLL_LOCKING and PLL_LOCKED mode bit[14:0] bucket size bit[15] ~ RSVD ~
0x41~0x42	[14:0]	NPLL_PHe_SOFT_TOLERANCE	R/W	0	NPLL's soft phase error tolerance. The phase error tolerance or re-entry from LOS/HOLDOVER mode. Unit in nS. bit[14:0] soft tolerance, unit(nS)
0x43~0x44	[14:0]	NPLL_PHe_HARD_TOLERANCE	R/W	0	NPLL's hard phase error tolerance. Phase error tolerance of the LOL thresh hold. Unit in nS. bit[14:0] hard tolerance, unit(nS)
0x45	[1:0]	NPLL_ALIGNED_PATH	R/W	0	NPLL's phase align configuration bit[0]: Phase aligned to 1PPS on XPLL: 1=YES, 0=NO bit[1]: Phase aligned to 1PPS on YPLL: 1=YES, 0=NO bit[2, 3]: DNC bit[4]: Align-in-Wide-Speed mode: 1=ON, 0=OFF bit[5]: NPLL_PD_CALI resolution: 1=COARSE, 0=FINE bit[7:6]: LEAKBUCK_FILL_RATE: rate=(n+1)=1~4 \<ps.1\> NPLL_PD_CALI resolution, see REG(NPLL_RT_PD_CALI) \<ps.2\> LEAKBUCK_FILL_RATE is used when the phase error is out of the threshold tolerance, otherwise, he leaking rate (=1) will be used.

ADDR	BITS	NAME	I/O	DEFAULT	DESCRIPTION
0x46~4B	[47:0]	NPLL_RT_ALIGNED_OUT_FREQ	R/W	0	The frequency of output to align to 1PPS output. Use the common division of the frequencies if more than 1 output. 17-bit. Unit in 8kHz. 　　bit [16:0]　　n, freq = 8kHz x n 　　bit [47:17]　　must be zero <ps.1> 　　Setting the aligned output frequency to zero means 1PPS output pulse does not need to phase align to any other clock outputs <ps.2> 　　This register used to be NPLL's configuration register and became NPLL's run-time register since firmware revision 0x03.
0x4C	[7:0]	NPLL_PHASE_SHIFT_SPEED	R/W	0	The maximal phase shifting speed to compensate the previous PBO (phase build-out) phase error while adjusting the phase alignment from FLL to PLL_FAST_LOCKING.. 　　Align-in-Wide-Speed mode is OFF: 　　　　bit[7:0] index=0~255; (band=0) 　　Align-in-Wide-Speed mode is ON: 　　　　bit[7:6] band=0~3 　　　　bit[5:0] index=0~63 　　maximal shift speed = index x (16band) x (10 pS/S)
0x4D~0x4E	[15:0]	NPLL_RT_PD_CALI	R/W	0	User specified phase detector offset calibration, to cover 1PPS input's quantization error and cable latency delay. 16-bit 2's complement. 　　- if NPLL_RT_PD_CALI resolution = FINE 　　　　- unit (2 pS), coverage = ± 65.536 nS 　　　　- cover more than 13-meter cable latency delay 　　- if NPLL_RT_PD_CALI resolution = COARSE 　　　　- unit(50 pS), coverage = ± 1.638 uS 　　　　- cover more than 300-meter cable latency delay
0x4F~0x54	[47:0]	NPLL_RT_MCLK_CALI	R/W	0	User specified MCLK frequency offset calibration. 28-bit 2's complement. Unit in (0.851495 ppt) 　　bit [27:0]　　calibration offset, 2's complement unit (0.851495 ppt) 　　bit [47:28]　　must be zero <ps.1> Writing a negative value will decrease the frequency. Writing a positive value will increase the frequency
0x55~0x5F		~ RSVD			
0x60~0x61	[12:0]	XPLL1_REF_FREQ_M	RW	1	NPLL synthesizes XPLL1's reference clock with frequency of (M *8kHz). 13-bit M value is set by this register. 　　1 <= M <= 5000
0x62		~ RSVD ~			
0x63~0x64	[14:0]	XPLL1_FB_DIV	RW	0	XPLL1 15-bit feedback divider value; Value 0 means disable
0x65	[0]	XPLL1_R0_SEL	RW	0	XPLL1 R0 selection, 　0　　Selection using Register XPLL1_R0_VALUE_L 　1　　Selection using Register XPLL1_R0_VALUE_S
0x66	[4:0]	XPLL1_R0_VALUE_S	RW	0	XPLL1 R0 value selection S. R0 is a combined resistor constituted of smaller resistors in series. Each bit controls one small resistor. Unit in ohm. 　　Bit0　0: 0.4k, 1: 2.5k 　　Bit1　0: 0.4k, 1: 5k 　　Bit2　0: 0.4k, 1: 10k 　　Bit3　0: 0.4k, 1: 20k 　　Bit4　0: 0.4k, 1: 40k

ADDR	BITS	NAME	I/O	DEFAULT	DESCRIPTION
0x67~0x68	[8:0]	XPLL1_R0_VALUE_L	RW	0	XPLL1 R0 value selection L. R0 is a combined resistor constituted of smaller resistors in series. Each bit controls one small resistor. Unit in ohm. Bit0 0: 1k, 1: 10k Bit1 0: 1k, 1: 20k Bit2 0: 1k, 1: 40k Bit3 0: 1k, 1: 80k Bit4 0: 1k, 1: 160k Bit5 0: 1k, 1: 320k Bit6 0: 1k, 1: 640k Bit7 0: 1k, 1: 1280k Bit8 0: 1k, 1: 2560k
0x69	[3:0]	XPLL1_R2	RW	0	XPLL1 R2 Value (160k ohm) / reg_value
0x6A~0x6B	[11:0]	XPLL1_CP_CURRENT	RW	0	XPLL1 charge pump current Current = 0.3125uA * reg_value
0x6C~0x6F		~ RSVD ~			
0x70	[2:0]	XPLL2_Pre_DIV	RW	0	The 3-bit divider value of the frequency pre-divider in front of XPLL2's PFD; Value 0 means disable
0x71	[6:0]	XPLL2_FB_DIV	RW	0	XPLL2 7-bit feedback divider value; Value 0 means disable
0x72	[0]	XPLL2_K$_{VCO}$	RW	0	XPLL2 K$_{VCO}$ 0 K$_{VCO}$ = K$_{small}$ = 22k ppm/volt 1 K$_{VCO}$ = K$_{large}$ = 33k ppm/volt
0x73	[0]	XPLL2_C0	RW	0	XPLL2 C0 value 0 100 pF 1 200 pF
0x74	[3:0]	XPLL2_R0	RW	0	XPLL2 R0 Value. Unit in ohm. 0:3k, 1:4.2k, 2:6k, 3:8.4k, 4:12k, 5:16.8k, 6:12k, 7:16.8k, 8:24k, 9:33.6k, 10:24k, 11:33.6k, 12:46.3k, 13:66k, 14:46.3k, 15:66k
0x75~0x76	[10:0]	XPLL2_CP_CURRENT	RW	0	XPLL2 charge pump current value; unit(1.25uA)
0x77~0x7F		~ RSVD ~			
0x80~0x81	[12:0]	YPLL1_REF_FREQ_M	RW	1	NPLL synthesizes YPLL1's reference clock with frequency of (M *8kHz). 13-bit M value is set by this register. 1 <= M <= 5000
0x82		~ RSVD ~			
0x83~0x84	[14:0]	YPLL1_FB_DIV	RW	0	YPLL1 15-bit feedback divider value; Value 0 means disable
0x85	[0]	YPLL1_R0_SEL	RW	0	YPLL1 R0 selection, 0 Selection in Reg YPLL1_R0_VALUE_L 1 Selection in Reg YPLL1_R0_VALUE_S
0x86	[4:0]	YPLL1_R0_VALUE_S	RW	0	YPLL1 R0 value selection S. R0 is a combined resistor constituted of smaller resistors in series. Each bit controls one small resistor. Unit in ohm. Bit0 0: 0.4k, 1: 2.5k Bit1 0: 0.4k, 1: 5k Bit2 0: 0.4k, 1: 10k Bit3 0: 0.4k, 1: 20k Bit4 0: 0.4k, 1: 40k
0x87~0x88	[8:0]	YPLL1_R0_VALUE_L	RW	0	YPLL1 R0 value selection L. R0 is a combined resistor constituted of smaller resistors in series. Each bit controls one small resistor. Unit in ohm. Bit0 0: 1k, 1: 10k Bit1 0: 1k, 1: 20k Bit2 0: 1k, 1: 40k Bit3 0: 1k, 1: 80k Bit4 0: 1k, 1: 160k Bit5 0: 1k, 1: 320k Bit6 0: 1k, 1: 640k Bit7 0: 1k, 1: 1280k Bit8 0: 1k, 1: 2560k

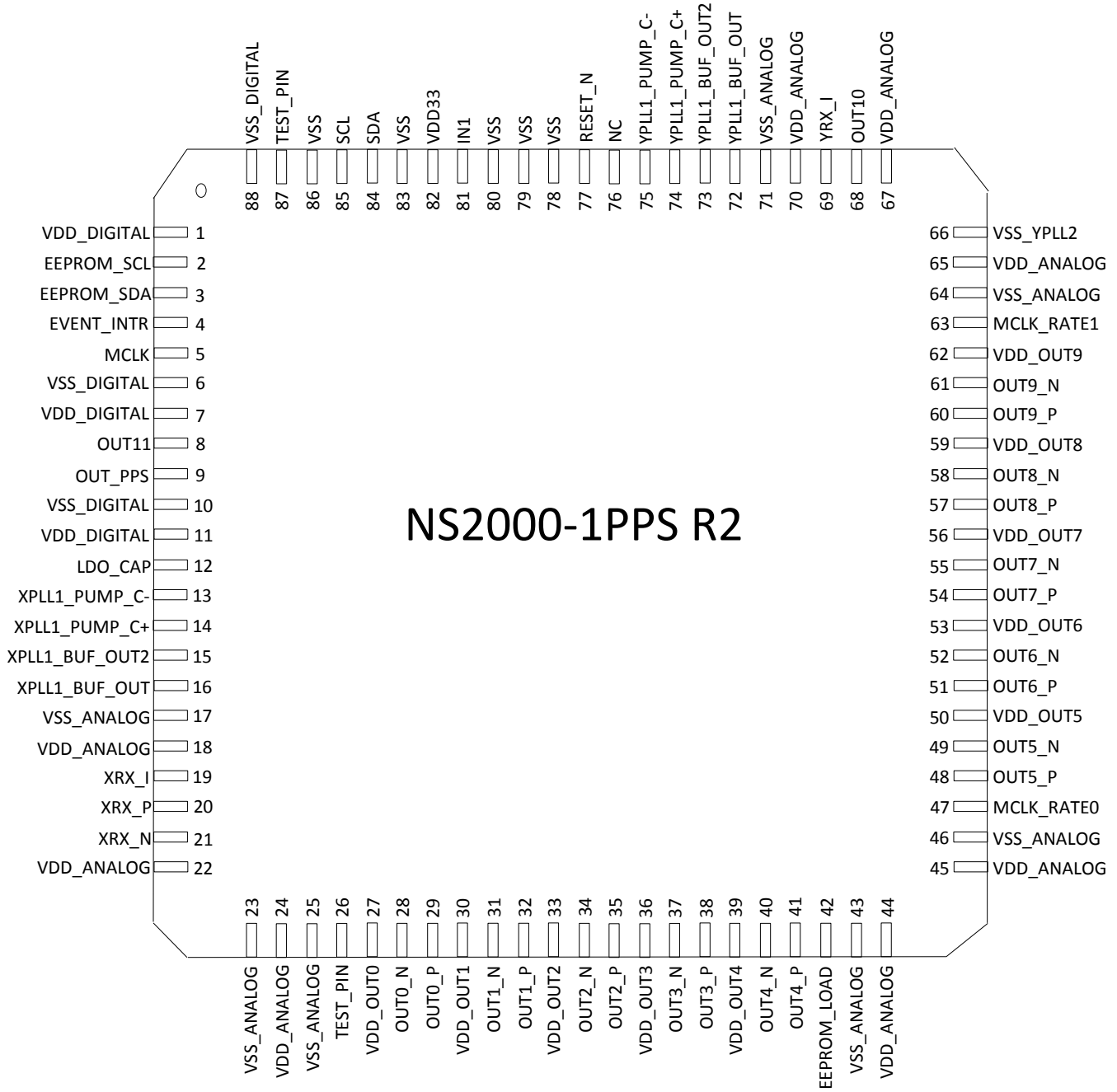| ADDR	BITS	NAME	I/O	DEFAULT	DESCRIPTION
0x89	[3:0]	YPLL1_R2	RW	0	YPLL1 R2 Value 160k ohm / reg_value
0x8A~0x8B	[11:0]	YPLL1_CP_CURRENT	RW	0	YPLL1 charge pump current Current = 0.3125uA * reg_value
0x8C~0x8F		~ RSVD ~			
0x90	[2:0]	YPLL2_Pre_DIV	RW	0	The 3-bit divider value of the frequency pre-divider in front of YPLL2's PFD; Value 0 means disable
0x91	[6:0]	YPLL2_FB	RW	0	YPLL2 7-bit feedback divider value; Value 0 means disable
0x92	[0]	YPLL2_KVCO	RW	0	YPLL2 K_{VCO} 0 $K_{VCO} = K_{small}$ = 22k ppm/volt 1 $K_{VCO} = K_{large}$ = 33k ppm/volt
0x93	[0]	YPLL2_C0	RW	0	YPLL2 C0 value 0 100 pF 1 200 pF
0x94	[3:0]	YPLL2_R0	RW	0	YPLL2 R0 Value. Unit in ohm 0: 3k, 1: 4.2k, 2: 6k, 3: 8.4k, 4:12k, 5: 16.8k, 6: 12k, 7: 16.8k, 8: 24k, 9: 33.6k, 10: 24k, 11: 33.6k , 12: 46.3k, 13: 66k, 14: 46.3k, 15: 66k
0x95~0x96	[10:0]	YPLL2_CP_CURRENT	RW	0	YPLL2 charge pump current value; unit(1.25uA)
0x97~0x9F		~ RSVD ~			
0xA0~0xA1	[11:0]	1PPS_PULSE_WIDTH	RW	10	1PPS output pulse width. Unit in uS.
0xA2	[3:0]	XPLL_ALIGN_PORT	RW	0	Select which output port sourced by XPLL to fine skew align to 1PPS output 0,9~15 alignment not required 1~8 Output 1~8
0xA3	[3:0]	YPLL_ALIGN_PORT	RW	0	Select which output port sourced by YPLL to fine skew align to 1PPS output Same as REG(XPLL_ALIGN_PORT)
0xA4	[0]	XPLL_OUT_SOURCE	RW	0	XPLL output source 0 XPLL1 1 XPLL2
0xA5	[0]	YPLL_OUT_SOURCE	RW	0	YPLL output source 0 YPLL1 1 YPLL2
0xA6	[2:0]	OUT_SOURCE_SEL	RW	0	Output 1~8 source selection, output can come from either XPLL or YPLL, the arrangement are as follows, 0,5,6,7 XPLL -> Output 1~8, YPLL -> none 1 XPLL -> Output 1~6, YPLL -> Output 7~8 2 XPLL -> Output 1~4, YPLL -> Output 5~8 3 XPLL -> Output 1~2, YPLL -> Output 3~8 4 XPLL -> none, YPLL -> Output 1~8
0xA7~0xA8	[13:0]	OUT11_SYNTH_FREQ			14-bit frequency value M for OUT11's synthesizer. Synthesizer Frequency = 8kHz * M , where 1,250 <= M <= 10,000, , 0: disable , 1~1249: writing will be ignored
0xA9~0xAA		~ RSVD ~			
0xAB~0xAF		~ RSVD ~			
0xB0	[4:0]	OUT0_TX_Mode	RW	0	Output0 transmitter mode, Bit[2:0] 0,6,7 power down the output driver 1 LVDS 2 LVPECL 3 LVCMOS, P on, N off 4 LVCMOS, P off, N on 5 LVCMOS, P on, N on When transmitter inw LVCMOS mode, bit[4:3] control polarity of output Bit[3] 0: P is not inverse, 1: P is inverse Bit]4] 0: N is not inverse, 1: N is inverse

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ADDR	BITS	NAME	I/O	DEFAULT	DESCRIPTION
0xB1	[4:0]	OUT1_TX_Mode			Output1 transmitter mode; Same as Output0 Transmitter Mode
0xB2	[4:0]	OUT2_TX_Mode	RW	0	Output2 transmitter mode; Same as Output0 Transmitter Mode
0xB3	[4:0]	OUT3_TX_Mode	RW	0	Output3 transmitter mode; Same as Output0 Transmitter Mode
0xB4	[4:0]	OUT4_TX_Mode	RW	0	Output4 transmitter mode; Same as Output0 Transmitter Mode
0xB5	[4:0]	OUT5_TX_Mode	RW	0	Output5 transmitter mode; Same as Output0 Transmitter Mode
0xB6	[4:0]	OUT6_TX_Mode	RW	0	Output6 transmitter mode; Same as Output0 Transmitter Mode
0xB7	[4:0]	OUT7_TX_Mode	RW	0	Output7 transmitter mode; Same as Output0 Transmitter Mode
0xB8	[4:0]	OUT8_TX_Mode	RW	0	Output8 transmitter mode; Same as Output0 Transmitter Mode
0xB9	[4:0]	OUT9_TX_Mode	RW	0	Output9 transmitter mode; Same as Output0 Transmitter Mode
0xC0~0xC2	[19:0]	OUT1_DIV	RW	0	20-bit OUTPUT1 divider value; Value 0 means divider disable; Value 1 means bypassing the divider
0xC3~0xC5	[19:0]	OUT2_DIV	RW	0	20-bit OUTPUT2 divider value; Value 0 means divider disable
0xC6~0xC8	[19:0]	OUT3_DIV	RW	0	20-bit OUTPUT3 divider value; Value 0 means divider disable; Value 1 means bypassing the divider
0xC9~0xCB	[19:0]	OUT4_DIV	RW	0	20-bit OUTPUT4 divider value; Value 0 means divider disable
0xCC~0xCE	[19:0]	OUT5_DIV	RW	0	20-bit OUTPUT5 divider value; Value 0 means divider disable
0xCF~0xD1	[19:0]	OUT6_DIV	RW	0	20-bit OUTPUT6 divider value; Value 0 means divider disable; Value 1 means bypassing the divider
0xD2~0xD4	[19:0]	OUT7_DIV	RW	0	20-bit OUTPUT7 divider value; Value 0 means divider disable
0xD5~0xD7	[19:0]	OUT8_DIV	RW	0	20-bit OUTPUT8 divider value; Value 0 means divider disable; Value 1 means bypassing the divider
0xD8~0xFF		~ RSVD ~			

Sub-Register Table of EEPROM/LOADING

ADDR	BITS	NAME	I/O	DEFAULT	DESCRIPTION
0xF0	[0]	EE_STS	R		EEPROM status 0: not ready 1: ready
0xF1~0xF2	[15:0]	EE_PAGE_IDX	RW	0	9-bit EEPROM page index, (1 page = 64-byte) bit[15] must be 0 bit[14:6] page index bit[6:9] must be 0b000000
0xF3	[7:0]	EE_FIFO	RW	0	8-bit EEPROM read/write FIFO port to 1 page (= 64-byte) FIFO buffer
0xF4	[1:0]	EE_CMD	RW	0	EEPROM command 0: reset FIFO pointer 1: load 1-page data from EEPROM to 64-byte FIFO buffer 2: burn 1-page data from FIFO buffer to EEPROM 3: ~ RSVD ~
0xF5~0xF6		~ RSVD ~			
0xF8	[7:0]	SOFT_RESET	W		To soft-reset this IC by writing 0xA5 into this register
0xF8	[0]	LOAD_STS	R		OTP/EEPROM Loading status 0: not complete 1: complete
0xF9	[1:0]	LOAD_CRC_STS	R		Loader Checksum status bit[0]: CONFIG 0:FAILED, 1:PASSED bit[1]: CODE 0:FAILED, 1:PASSED
0xFA~0xFF		~ RSVD ~			

NS2000-1PPS Pin Assignments (Top View)

NS2000-1PPS R2

Top pins (88–67): VSS_DIGITAL (88), TEST_PIN (87), VSS (86), SCL (85), SDA (84), VSS (83), VDD33 (82), IN1 (81), VSS (80), VSS (79), VSS (78), RESET_N (77), NC (76), YPLL1_PUMP_C- (75), YPLL1_PUMP_C+ (74), YPLL1_BUF_OUT2 (73), YPLL1_BUF_OUT (72), VSS_ANALOG (71), VDD_ANALOG (70), YRX_I (69), OUT10 (68), VDD_ANALOG (67)

Left pins (1–22):
1 VDD_DIGITAL
2 EEPROM_SCL
3 EEPROM_SDA
4 EVENT_INTR
5 MCLK
6 VSS_DIGITAL
7 VDD_DIGITAL
8 OUT11
9 OUT_PPS
10 VSS_DIGITAL
11 VDD_DIGITAL
12 LDO_CAP
13 XPLL1_PUMP_C-
14 XPLL1_PUMP_C+
15 XPLL1_BUF_OUT2
16 XPLL1_BUF_OUT
17 VSS_ANALOG
18 VDD_ANALOG
19 XRX_I
20 XRX_P
21 XRX_N
22 VDD_ANALOG

Right pins (66–45):
66 VSS_YPLL2
65 VDD_ANALOG
64 VSS_ANALOG
63 MCLK_RATE1
62 VDD_OUT9
61 OUT9_N
60 OUT9_P
59 VDD_OUT8
58 OUT8_N
57 OUT8_P
56 VDD_OUT7
55 OUT7_N
54 OUT7_P
53 VDD_OUT6
52 OUT6_N
51 OUT6_P
50 VDD_OUT5
49 OUT5_N
48 OUT5_P
47 MCLK_RATE0
46 VSS_ANALOG
45 VDD_ANALOG

Bottom pins (23–44): VSS_ANALOG (23), VDD_ANALOG (24), VSS_ANALOG (25), TEST_PIN (26), VDD_OUT0 (27), OUT0_N (28), OUT0_P (29), VDD_OUT1 (30), OUT1_N (31), OUT1_P (32), VDD_OUT2 (33), OUT2_N (34), OUT2_P (35), VDD_OUT3 (36), OUT3_N (37), OUT3_P (38), VDD_OUT4 (39), OUT4_N (40), OUT4_P (41), EEPROM_LOAD (42), VSS_ANALOG (43), VDD_ANALOG (44)

Pin Connection Recommendations

- VCC Pins and Decoupling: all VCC pins must always be connected.
- Unused Clock Outputs: leave unused clock outputs floating and powered down.
- Unused XRX and YRX input pins can be left floating and powered down.

NS2000-1PPS Pin Description

Pin No.	Pin Name	I/O	Description
1	VDD_DIGITAL	Power	3.3V digital power input
2	EEPROM_SCL	I	Serial Clock Input from external EEPROM load
3	EEPROM_SDA	I/O	Serial Data from external EEPROM load
4	EVENT_INTR	I	Event Interrupt
5	MCLK	I	Master clock input (e.g., OCXO or TCXO) 10MHz or 20MHz 3.3V LVCMOS
6	VSS_DIGITAL	Power	Digital Ground
7	VDD_DIGITAL	Power	3.3V analog power input
8	OUT11	O	LVCMOS clock output CLK11. 1kHz to 156.25MHz, in 1kHz steps
9	OUT_1PPS	O	1PPS clock pulse output
10	VSS	Power	Digital Ground
11	VDD33	Power	3.3V analog power input
12	LDO_CAP		Connect internal LDO to external MLCC capacitor to GND (~1 uF) *Note: keep trace very short between IC and Cap*
13	XPLL1_PUMP_C-		Connect to APLL's external filter –)
14	XPLL1_PUMP_C+		Connect internal LDO to output capacitor
15	XPLL1_BUF_OUT2		Connect to VCXO voltage control pin (optional connecting to cap
16	XPLL1_BUF_OUT		Connect to VCXO voltage control pin (optional connecting to cap)
17	VSS_ANALOG	Power	Analog ground
18	VDD_ANALOG	Power	3.3V analog power input
19	XRX_1	I	Accepts single ended clock /VCXO's 3.3V LVCMOS clock output
20	XRX_P	I	Accept XO or VCXO's 3.3V LVPECL/LVDS positive clock output
21	XRX_N	I	Accept XO or VCXO's 3.3V LVPECL/LVDS negative clock output
22	VDD_ANALOG	Power	3.3V analog power input
23	VSS_ANALOG	Power	Analog ground
24	VDD_ANALOG	Power	3.3V analog power input
25	VSS_ANALOG	Power	Analog ground
26	TEST_PIN		Do not connect
27	OUT0_N	O	Differential output 0 negative (LVPECL/LVDS) or LVCMOS (Bypass from VCXOx)
28	OUT0_P	O	Differential output 0 positive (LVPECL/LVDS) or LVCMOS (Bypass from VCXOx)
29	VDD_OUT0	Power	3.3V analog power input
30	VDD_OUT1	Power	3.3V analog power input
31	OUT1_N	O	Differential output 1 negative (LVPECL/LVDS) or LVCMOS
32	OUT1_P	O	Differential output 1 positive (LVPECL/LVDS) or LVCMOS
33	VDD_OUT2	Power	3.3V analog power input
34	OUT2_N	O	Differential output 2 negative (LVPECL/LVDS) or LVCMOS
35	OUT2_P	O	Differential output 2 positive (LVPECL/LVDS) or LVCMOS
36	VDD_OUT3	Power	3.3V analog power input
37	OUT3_N	O	Differential output 3 negative (LVPECL/LVDS) or LVCMOS
38	OUT3_P	O	Differential output 3 positive (LVPECL/LVDS) or LVCMOS
39	VDD_OUT4	Power	3.3V analog power input
40	OUT4_N	O	Differential output 4 negative (LVPECL/LVDS) or LVCMOS
41	OUT4_P	O	Differential output 4 positive (LVPECL/LVDS) or LVCMOS
42	EPROM LOAD	I	Active high to load firmware via external EEprom into pins 2 and 3.
43	VSS_ANALOG	Power	Analog ground
44	VDD_ANALOG	Power	Analog 3.3V power input
45	VDD_ANALOG	Power	Analog 3.3V power input
46	VSS_ANALOG	Power	Analog ground
47	MCLK_RATE0		Select MCLK frequency. 10MHz, 20MHz,19.2MHz, 24.576MHz
48	OUT5_P	O	Differential output 5 positive (LVPECL/LVDS) or LVCMOS
49	OUT5_N	O	Differential output 5 negative (LVPECL/LVDS) or LVCMOS
50	VDD_OUT5	Power	Analog 3.3V power input

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Pin No.	Pin Name	I/O	Description
51	OUT6_P	O	Differential output 6 positive (LVPECL/LVDS) or LVCMOS
52	OUT6_N	O	Differential output 6 negative (LVPECL/LVDS) or LVCMOS
53	VDD_OUT6	Power	Analog 3.3V power input
54	OUT7_P	O	Differential output 7 positive (LVPECL/LVDS) or LVCMOS
55	OUT7_N	O	Differential output 7 negative (LVPECL/LVDS) or LVCMOS
56	VDD_OUT7	Power	Analog 3.3V power input
57	OUT8_P	O	Differential output 8 positive (LVPECL/LVDS) or LVCMOS
58	OUT8_N	O	Differential output 8 negative (LVPECL/LVDS) or LVCMOS
59	VDD_OUT8	Power	Analog 3.3V power input
60	VDD_OUT9	Power	Analog 3.3V power input
61	OUT9_P	O	Differential output 9 positive (LVPECL/LVDS) or LVCMOS (Bypass from VCXOy)
62	OUT9_N	O	Differential output 9 negative (LVPECL/LVDS) or LVCMOS (Bypass from VCXOy)
63	MCLK_RATE1	I	Select MCLK frequency. 10MHz, 20MHz, 19.2MHz, 24.576MHz
64	VSS_ANALOG	Power	Analog ground
65	VDD_ANALOG	Power	Analog 3.3V power input
66	VSS_YPLL2	Power	Analog Ground
67	VDD_ANALOG	Power	3.3V power input YPLL2
68	OUT10	0	Output of YRX_1 Signal
69	YRX_I	I	Accept XO or VCXO's 3.3V LVCMOS clock output
70	VDD_ANALOG	Power	Analog 3.3V power input
71	VSS_ANALOG	Power	Analog ground
72	YPLL1_BUF_OUT		Connect to VCXO voltage control pin (optional connecting to cap)
73	YPLL1_BUF_OUT2		Connect to VCXO voltage control pin (optional connecting to cap)
74	YPLL1_PUMP_C+		Connect to APLL's external filter
75	YPLL1_PUMP_C-		Connect to APLL's external filter
76	VPP	N/C	For factory programming of internal OTP
77	RESET_N	I	Resets chip. Active Low, internally pulled up high.
78	VSS	Power	Digital Ground
79	VSS	Power	Digital Ground
80	VSS	Power	Digital Ground
81	IN1	I	Reference input accepts 1PPS
82	VDD33	Power	Digital 3.3V power input
83	VSS	Power	Digital Ground
84	SDA		SPI bus data output
85	SCL		SPI bus data intput
86	VSS	Power	Digital Ground
87	TEST_PIN		Do not connect
88	VDD_DIGITAL	Pwr	3.3V power input YPLL0

Notes on Pin Description

RESET_N

Pin RESET_N is an I/O input pin used to initiate a "hard" reset to the IC. The RESET_N pin is internally "pulled-high". Driving this pin "Low" for at least 1uS and releasing it, or driving it "High" again will reset the device. The IC will be ready to access through the control bus interface in 10 mS after the reset operation.

In addition to the RESET_N hardware pin reset function, a SOFT_RESET reboot option exists in the IC's internal design. The register "SOFT_RESET" at 0 xA5 is a write-only register. Similar to the hard reset, once the register is written to, the IC's registers will be ready to access through the control bus interface after 10mS.

Both the hard reset and the soft reset will cause the IC to reboot. The reboot procedure will first reload the content from the internal OTP. If the EEPROM_LOAD pin is tied "high", an external EEPROM's content will be loaded into the IC after the OTP content is loaded. Only the hard reset procedure will check the MCLK_RATE0 and MCLK_RATE1 to determine the clock frequency of the MCLK input.

This IC has a built-in power-on-reset (POR) circuit. However, a hard reset may need to be initiated if the supplied voltage to the IC has a very slow rising rate.

EEPROM_LOAD

EEPROM OPERATION: This IC supports the use of an external EEPROM to load firmware or default values of all read/write registers. This function is intended primarily to provide the ability for "field upgrade" flexibility to update firmware (Code+Data). Using an external EEPROM may also be considered for loading the default values of the read/write registers in preference to using the OTP memory. However, EEPROM content cannot be used to change the default values of read-only registers. CRC16 checksum protection is supported.

EEPROM BOOTING: The IC will always boot from the internal OTP content first. If the pin EEPROM_LOAD is tied "HIGH", the IC will continue to download content from the EEPROM to override the OTP's content during the boot-up stage. This procedure will be triggered after both a power cycle and a reset procedure (Hard or Soft).

EEPROM CONNECTION: This IC has an I2C master control dedicated to read/write data from a specific I2C EEPROM. The ATMEL AT24C256C (256-kbit I2C EEPROM IC) is required for use with this IC. For connection:

    EEPROM's I2C address ended with 0b000
- Ties pin A0, A1, A2 to ground

    Disable write protection
- Ties pin WP to ground

    Connect to this IC
- Tie pin SCL to this IC's pin EEPROM_SCL
- Tie pin SDA to this IC's pin EEPROM_SDA
- Data rate will be 1MHz (if traces are too long, some termination may be required)

EEPROM UPDATE OPERATION FROM USERS: This IC supports I2C bus interface as a control interface. This means the user can read/write content from/to the external EEPROM from this IC.

The EEPROM operations registers on this IC are:
- REG (EE_STS)
- REG (EE_PAGE_IDX)
- REG (EE_FIFO)
- REG (EE_CMD)

    EEPROM content image
- Image size = 18,048 bytes
- Image content will be provided by manufacturer
- Each EEPROM image will be presented by an 18,048-byte long binary file
- Image integrity is protected by industry-grad CRC16 checksum

    EEPROM Read/Write Operation
- Both read/write operation is in 64-byte page orientation
- The 18,048-byte binary image will be separated into 282 64-byte pages, indexed from 0 to 281

    Page WRITE operation example:
- Wait until EE_STS indicates it is "ready"
- Setup the corresponding page index
- Issue FIFO pointer reset command
- Issue FIFO-read-from-EEPROM command
- Wait until EE_STS indicates it is ready
- Read the 64 byte page content from the FIFO port, in the order from LSB byte
- After updating the EEPROM content, read them back to ensure no corrupt data was generated during the read/write operation.

Notes on Pin Description continued

EEPROM_LOAD continued

Page READ operation example:

- Wait until EE_STS indicates IC is "ready"
- Setup the corresponding page index
- Issue FIFO pointer reset command
- Issue FIFO-read-from-EEPROM command
- Wait until EE_STS indicates IC is ready
- Read the 64 byte page content from the FIFO port, in the order from LSB to MSB byte
- After updating the EEPROM content, read them back to ensure no corrupt data was generated during the read/write operation.

CONTROL -BUS OPERATION

The control bus type of this IC uses a standard I2C interface. The I2 C interface has the advantage of requiring only two control pins and is a de facto standard throughout the I2C industry. The I2C port consists of a serial data line (SDA) and a serial clock line (SCL). In an I2C bus system, the NS2000 is connected to the serial bus (data bus SDA and clock bus SCL) as a slave device; that is, no clock is generated by the NS2000. The NS2000 uses direct 8-bit memory addressing.

Users can read/write registers through this control bus. The I2C slave controller does not support multi-master operation. Supporting clock rate is up to 1MHz.

The fixed I2C address is: Slave address = 0b101.0001

I2C frame and data transfer format-

This IC supports a 7-bit I2C address (slave address = 0b101.0001). The format is MSB-bit leading. This format uses only one byte for the 8-bit RAM/REG address. When read/write in burst mode (i.e. more than one data byte in an I2C frame), the RAM/REG address will be increased by one automatically for each data byte.

Multi-Byte Register Operation-

This IC has many registers. Some of these registers are a single byte and some are a multi-byte format. A Register's address is in unit of byte. For each multi-byte register, it forms in LSB (least significant byte) first order. The LSB byte shall have a lower address. When read/write to a multi-byte register, you must always access in the order from LSB byte to MSB byte. You should not interrupt a multi-byte register read/write with other bus operations. The writing to a multi-byte register will take effect when you are writing its MSB byte.

Reference ITU-T Recommendations

|	
G.781	Synchronization layer functions
G.8261	Timing and Synchronization aspects in Packet Networks
G.8262	Timing characteristics of synchronous Ethernet Equipment slave clock (EEC)
G.8264	Distribution of timing through packet networks
G.8251	The control of jitter and wander within the optical transport network (OTN)
G.8265	Architecture and requirements for packet based frequency delivery
G.8265.1	ITU-T profile for frequency distribution without timing support from the network
G.8261.1, G.8271, G.8272, G.8273, G.8273.1, G.8273.2, G.8273.3, G.8275	

88 Pin QFN Package (10 x 10mm)

Package Dimensions

TOP VIEW

SIDE VIEW
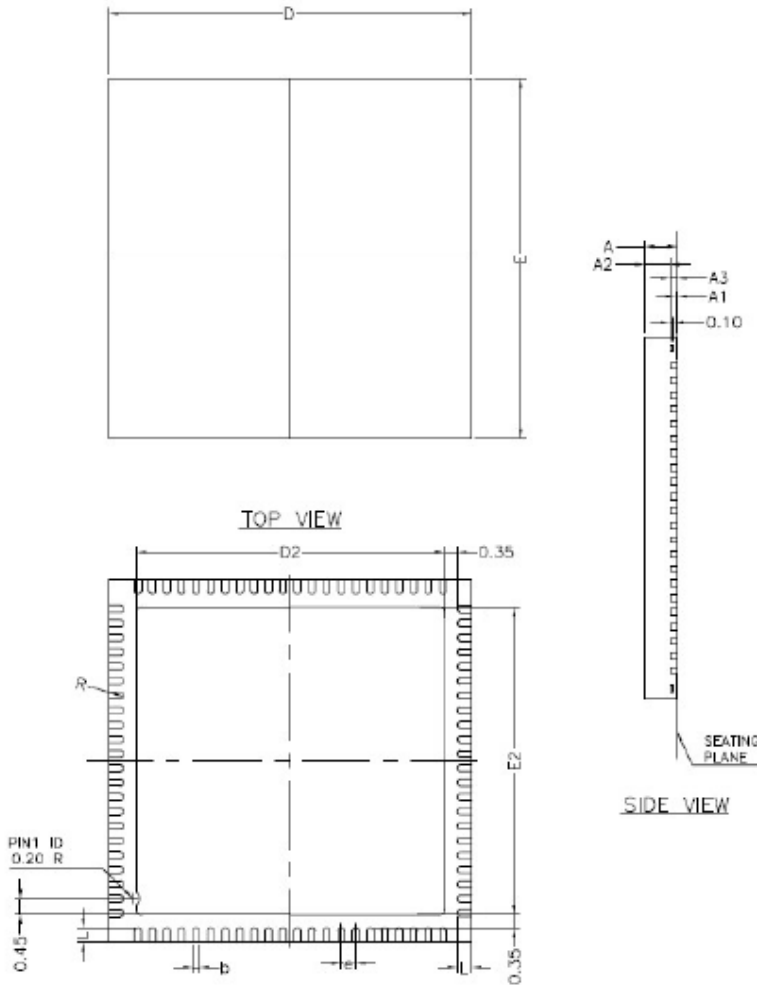
Table of Dimensions

SYMBOL	MILLIMETER		
	MIN.	NOM.	MAX.
A	0.80	0.85	0.90
A1	0.00	0.035	0.05
A2	—	0.65	0.70
A3	0.203 REF		
b	0.13	0.18	0.23
D	10.00 BSC		
D2	8.40	8.50	8.60
E	10.00 BSC		
E2	8.40	8.50	8.60
e	0.40 BSC		
L	0.35	0.40	0.45
R	0.065	—	—

Notes

1. Conforms to JEDEC standard JESD-30 MO220.

2. Side of body may be square or curved.

3. Exposed pad may have chamfer in area of Pin 1

Layout Recommendations

The printed circuit board that houses the NS2000-1PPS should be designed so that the analog and digital sections are separated and confined to certain areas of the board. This facilitates the use of ground planes that can be easily separated. A minimum etch technique is generally best for ground planes because it gives the best shielding. Digital and analog ground planes should be joined in only one place. If the NS2000-1PPS is the only device requiring an AGND-to-DGND connection, then the ground planes should be connected at the AGND and DGND pins of the NS2000-1PPS. If the NS2000-1PPS is in a system where multiple devices require AGND-to-DGND connections, the connection should be made at one point only, a star ground point that should be established as close as possible to the NS2000-1PPS.

Avoid running digital lines under the device because these couple noise onto the die. The analog ground plane should run under the NS2000-1PPS to avoid noise coupling. The power supply lines to the NS2000-1PPS should use as large a track as possible to provide low impedance paths and reduce the effects of glitches on the power supply line. Fast switching signals, such as clocks, should be shielded with digital ground to avoid radiating noise to other sections of the board. Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other, reducing the effects of feed-through. A micro-strip technique is by far the best but is not always possible with a double-sided board. In this technique, the component side of the board is dedicated to ground planes, while signals are placed on the other side.

Good decoupling is important. The analog and digital supplies to the NS2000-1PPS are independent and separately pinned out to minimize coupling between analog and digital sections of the device. All analog and digital supplies should be decoupled to AGND and DGND, respectively, with 0.1 µF ceramic capacitors in parallel with 10 µF tantalum capacitors. To achieve the best from the decoupling capacitors, they should be placed as close as possible to the device, ideally right up against the device. In systems where a common supply is used to drive both the AVDD and DVDD of the NS2000-1PPS, it is recommended that the system's AVDD supply be used. This supply should have the recommended analog supply decoupling between the AVDD pin of the NS2000-1PPS and AGND and the recommended digital supply decoupling capacitors between the DVDD pin and DGND.

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Revision History

Revision	Date	Note
04	07/14/20	Updated EEPROM_LOAD Description
05	07/29/20	Updated Register 0x65 and 0x86
06	01/26/21	Update block diagram and register 0x4F~0x54 description.
07	02/16/21	Update Register and Pin Assignment Descriptions
08	02/18/21	Additional updates to Registry Table