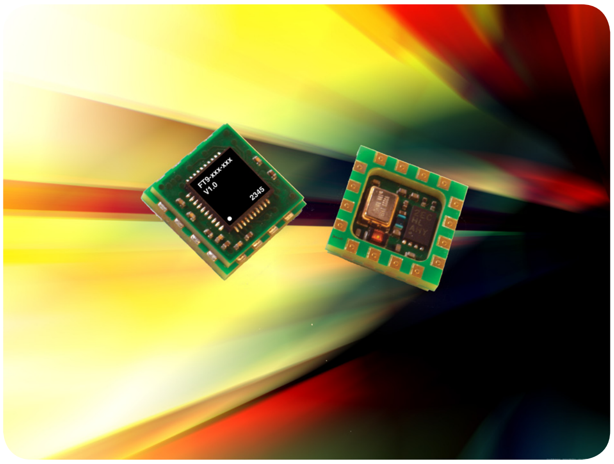
April 2025

Unlocking Precision Timing with the FT9-TFC GNSS Timing System

In today's precision timing applications, stability and accuracy are critical.



In today's precision timing applications, stability and accuracy are critical. The Connor Winfield FT9 TFC is a flexible 1PPS locking timing system that integrates a digital phase-locked loop (DPLL) with a numerically controlled oscillator (NCO) to offer exceptional synchronization capabilities. Its ability to leverage different master clock (MCLK) sources—ranging from a temperature-compensated crystal oscillator (TCXO) to various oven-controlled crystal oscillators (OCXO) or double OCXO (DOCXO)—allows users to optimize performance based on their specific needs.

This white paper explores the performance benefits of different MCLK configurations and loop bandwidth settings, highlighting their impact on frequency stability, phase noise, and holdover accuracy. Performance plots are provided to illustrate these distinctions, guiding users toward the best setup for their application.

Key Benefits of the FT9 TFC Timing System

- Flexible Master Clock Input: Supports onboard TCXO or external OCXO/DOCXO.
- Customizable Loop Bandwidth: Configurable bandwidth settings for optimal trade-offs between noise filtering and response time.
- Advanced Sawtooth Error Correction: Improves phase stability using quantization error messaging.
- Enhanced Holdover Performance: Maintains precise timing eve when GNSS signals are lost.

Understanding the Role of Loop Bandwidth and MCLK Sources with undisciplined 1PPS sources

Comparison of Configurations

The FT9 TFC provides many configuration options but three primary configurations are illustrated here, each being driven by a 1PPS reference input derived from GNSS receivers that have not been compensated for their sawtooth error, Ublox Neo-F10T and Ublox MAX M10S:

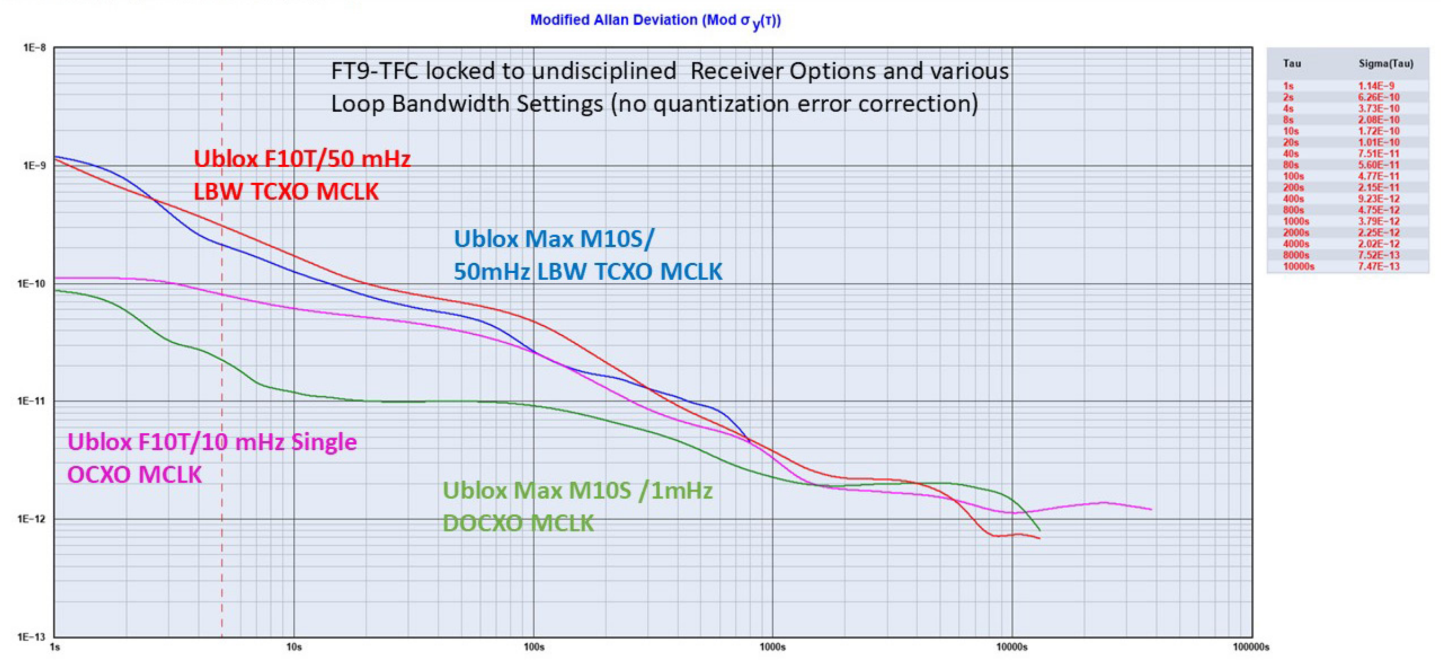
1. Neo F10T with TCXO MCLK and 50mHz Loop Bandwidth (LBW) – Fast response, high adaptability with higher phase noise.
2. MAX M10S with TCXO MCLK and 50mHz Loop Bandwidth (LBW) – Fast response, high adaptability with higher phase noise
3. NEO F10T with Single OCXO MCLK and 10mHz LBW – Superior holdover performance, reduced noise.
4. MAX M10S with DOCXO MCLK and 1 mHz LBW – Best overall stability, lowest phase noise.

MDEV Performance Comparison

MDEV Convergence Around 1000 Seconds: The convergence of the MDEV plots for all MCLK and LBW options around 1000 seconds occurs due to the transition from short-term frequency noise to long-term drift mechanisms. At shorter timescales (< 100s), high-frequency noise dominates, meaning that lower bandwidth settings and higher-quality oscillators (OCXO/DOCXO) perform significantly better. However, around 1000 seconds, the GNSS disciplining effect takes precedence, equalizing stability across all configurations. The loop bandwidth and oscillator quality have less impact in this region because the GNSS corrections begin to dominate frequency control.

Beyond 1000 seconds without GPS lock, the primary driver of stability becomes the oscillator's long-term drift and aging characteristics, which explains why holdover performance differs significantly when GNSS signals are unavailable. For applications requiring prolonged GNSS loss handling, a high precision DOCXO or OCXO with a 1.2mHz LBW setting remains the most stable choice.

- DOCXO with 1 mHz LBW demonstrates the lowest Modified Allan Deviation (MDEV), ensuring the highest frequency stability over time.
- Single OCXO configurations show progressively better stability than TCXO, with the 10 mHz LBW setting further reducing frequency fluctuations.
- TCXO exhibits the highest MDEV. With its 50mHz loop bandwidth setting, the FT9 system basically just follows the raw 1PPS performance from the receiver with minimal added filtering.



Tau	Sigma(Tau)
1s	1.14E-9
2s	6.26E-10
4s	3.73E-10
8s	2.08E-10
10s	1.72E-10
20s	1.01E-10
40s	7.51E-11
80s	5.60E-11
100s	4.77E-11
200s	2.15E-11
400s	9.23E-12
800s	4.75E-12
1000s	3.79E-12
2000s	2.25E-12
4000s	2.02E-12
8000s	7.52E-13
10000s	7.47E-13

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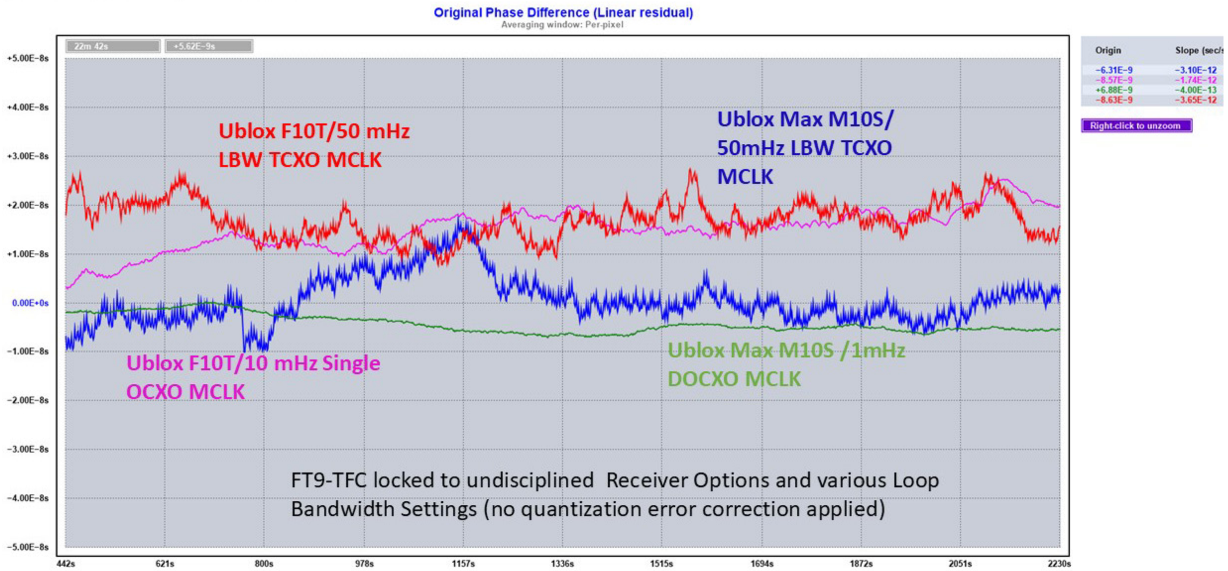
Phase Difference Comparison

Phase Difference and Locking Performance Phase coherence is a critical aspect of timing applications. The FT0-TFC's phase-locked loop (PLL) performance improves with lower bandwidth settings and more stable oscillators.

- TCXO with 50mHz LBW shows the highest residual phase error due to its increased sensitivity to short-term fluctuations. Both receiver options looked the same..
- Single OCXO with 6.4mHz LBW reduces phase deviations, while the 1.2mHz LBW setting provides even tighter phase control.
- DOCXO or OCXO with 1.2mHz LBW delivers the most consistent phase stability, ensuring minimal deviation over extended periods.



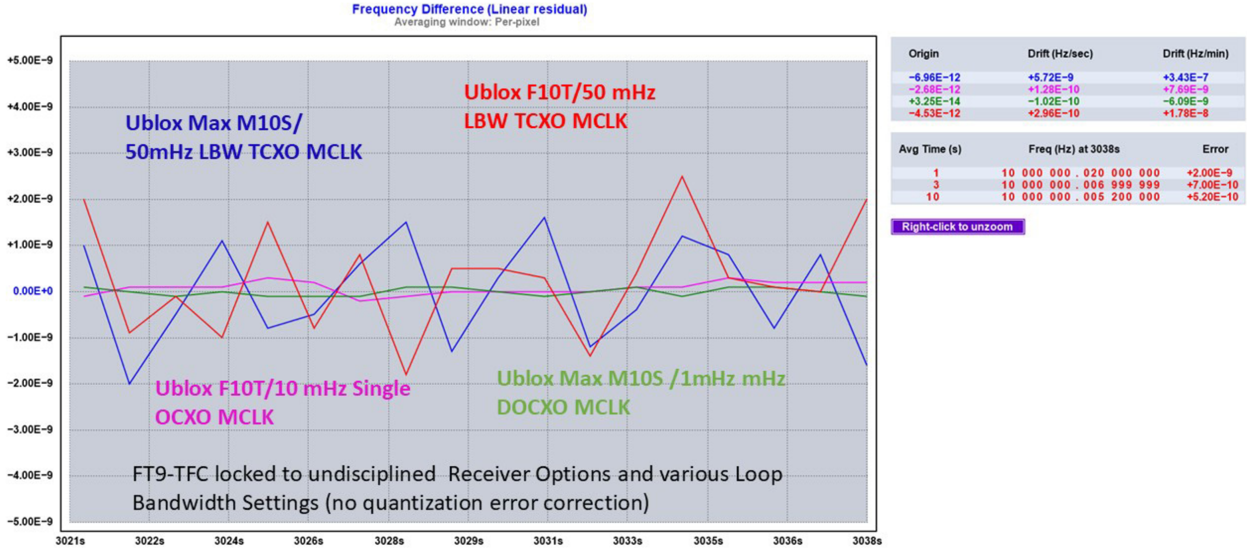
FT9-TFC locked to undisciplined Receiver Options and various Loop Bandwidth Settings (no quantization error correction applied)

Origin	Slope (sec/
−6.31E−9	−3.10E−12
−8.57E−9	−1.74E−12
+6.88E−9	−4.00E−13
−8.63E−9	−3.65E−12

Frequency Difference Comparison

Effect of Loop Bandwidth on Short-Term Frequency Fluctuations and Its Relationship to Frequency Difference Measurements.

- With minimal filtering and no phase compensation for quantization error (sawtooth error), short term frequency fluctuations remain high.
- Lower bandwidth settings with single OCXO at 10mHz LBW exhibit greatly reduced frequency fluctuations, leading to improved short term frequency stability, even without phase compensation for quantization error.
- DOCXO with 1mHz LBW provides the least variation in short-term frequency.
- TCXO with 50mHz LBW exhibits more variation, showing higher short term instability for either receiver model.



FT9-TFC locked to undisciplined Receiver Options and various Loop Bandwidth Settings (no quantization error correction)

Origin	Drift (Hz/sec)	Drift (Hz/min)
−6.96E−12	+5.72E−9	+3.43E−7
−2.68E−12	+1.28E−10	+7.69E−9
+3.25E−14	−1.02E−10	−6.09E−9
−4.53E−12	+2.96E−10	+1.78E−8

Avg Time (s)	Freq (Hz) at 3038s	Error
1	10 000 000 . 020 000 000	+2.00E−9
3	10 000 000 . 006 999 999	+7.00E−10
10	10 000 000 . 005 200 000	+5.20E−10

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Why Phase and Frequency Difference Measurements Reduce Proportionally to Loop Bandwidth setting reductions

The observed reduction in phase and frequency and difference measurements as loop bandwidth decreases is a direct consequence of how the phase-locked loop (PLL) filters noise and responds to frequency fluctuations:

- Filtering of High-Frequency Noise: A lower loop bandwidth acts as a low-pass filter, significantly attenuating high-frequency variations that contribute to short-term frequency fluctuations. This results in a smoother frequency output, minimizing deviations in the frequency difference measurements.
- Reduced Response to GNSS Jitter: A wider bandwidth setting allows the PLL to react more quickly to GNSS timing variations, leading to more frequent but smaller frequency corrections. Conversely, a narrower bandwidth setting slows down these corrections, preventing the PLL from introducing rapid variations in response to GNSS fluctuations.
- Increased Dependence on the Local Oscillator: At lower band widths, the PLL relies more on the intrinsic stability of the master clock (MCLK), especially in the presence of high-quality OCXO and DOCXO sources. Since these oscillators have inherently lower frequency noise, the frequency difference measurements show much smaller variations compared to a system with a TCXO and higher bandwidth.

Thus, as the loop bandwidth is reduced, the system shifts from a rapid correction mechanism (which increases frequency variation) to a more stable, oscillator-dependent system (which minimizes short-term frequency fluctuations). This explains why lower bandwidth settings produce proportionally smaller frequency difference measurements and why DOCXO configurations with narrow LBW settings exhibit the best frequency stability.

Understanding the Role of MCLK Sources at various Loop Bandwidth settings

Local Oscillator Requirements for Low Bandwidth Settings

The ability to successfully implement a low loop bandwidth setting, such as 1mHz, depends heavily on the quality of the master clock (MCLK). The local oscillator must meet stringent stability and noise performance requirements to ensure optimal phase lock loop (PLL) operation. Key considerations include:

- Phase Noise Performance: A high-quality OCXO or DOCXO with low phase noise ensures the PLL can operate effectively without excessive correction noise. A TCXO, with its higher phase noise, is unsuitable for very low bandwidth settings.
- Short-Term Stability: The Allan Deviation (ADEV) of the oscillator must be sufficiently low to prevent excessive phase fluctuations. Typical minimum requirements for 1mHz loop bandwidth include:
  - OCXO: ADEV in the range of 5×10^{12} at 1s.
  - DOCXO: ADEV in the range of 2×10^{12} at 1s.
- Thermal Stability: Temperature-induced frequency variations must be minimal. DOCXOs, with their tighter thermal compensation, perform best in this scenario.
- Aging Characteristics: Over extended periods, frequency drift must remain within acceptable limits. A high-quality DOCXO exhibits minimal drift, making it ideal for applications requiring long-term frequency accuracy.

The lower the loop bandwidth, the more the system depends on the stability of the MCLK rather than external GNSS corrections. Thus, a high-performance OCXO or DOCXO is essential for achieving reliable performance at 1mHz loop bandwidth, while TCXOs and lower-grade OCXOs are unsuitable due to their higher noise and drift characteristics.

Understanding the Role of Quantization Error Correction

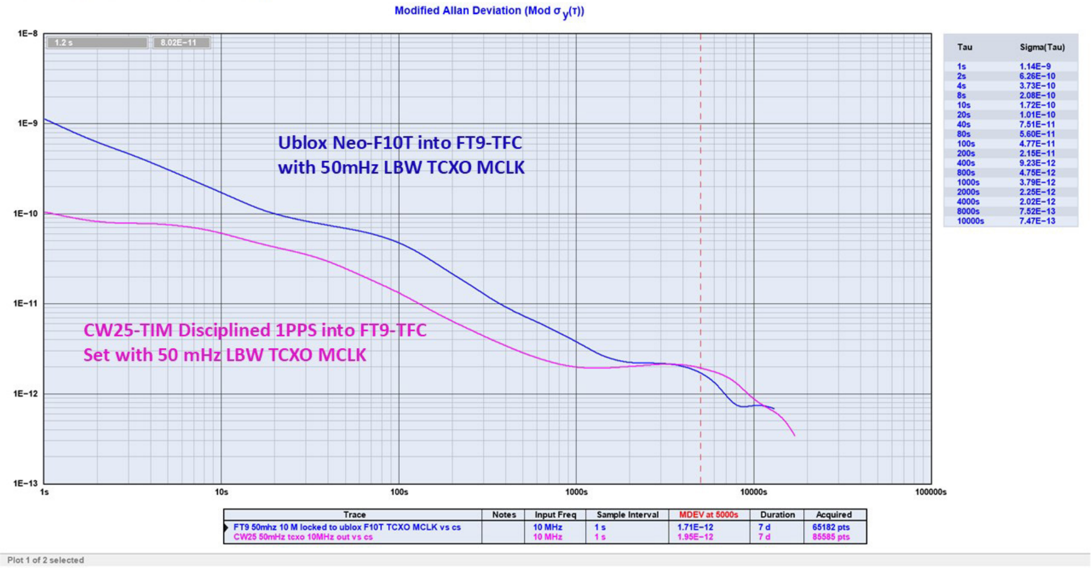
Advanced Sawtooth Error Compensation and PLL Stability is one of the FT9-TFC's standout features is its ability to correct for sawtooth errors using quantization error messaging and phase compensation control. By predicting the location of the next GNSS PPS pulse and adjusting the phase accordingly, the receiver enhances its PLL performance:

- Minimizing Phase Jitter: Active compensation smooths phase tracking, reducing noise artifacts.
- Enhancing Locking Performance: Predictive adjustments keep the PLL tightly locked.
- Reducing Frequency Drift: Improves holdover stability by maintaining a consistent frequency reference.

Comparison of Configurations with and without Quantization Error Compensation Implemented

The FT9 TFC provides many configuration options but one configuration is illustrated here to show the effect of quantization error correction in the 1PPS output. In this illustration, we compare a Ublox Neo-F10T undisciplined 1PPS versus a 1PPS disciplined and output by the CW25-TIM, both going into the FT9-TFC using a TCXO MCLK set with a 50mHz loop bandwidth.

MDEV Performance Comparison



Tau	Sigma(Tau)
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40s	7.51E−11
80s	5.60E−11
100s	4.77E−11
200s	2.15E−11
400s	9.23E−12
800s	4.75E−12
1000s	3.79E−12
2000s	2.25E−12
4000s	2.02E−12
8000s	7.52E−13
10000s	7.47E−13

Trace	Notes	Input Freq	Sample Interval	MDEV at 5000s	Duration	Acquired
FT9 50mhz 10 M locked to ublox F10T TCXO MCLK vs cs		10 MHz	1 s	1.71E−12	7 d	65182 pts
CW25 50mHz tcxo 10MHz out vs cs		10 MHz	1 s	1.95E−12	7 d	85585 pts

- TCXO MLCK with 50mHz LBW setting supports "lock" condition on the 1PPS of both receiver options, but the MDEV performance looks dramatically different.
- Using the same 50mHz loop bandwidth setting shows markedly improved results when implementing quantization error correction versus the raw 1PPS directly from a "good" timing receiver like the Ublox 10 series specified with a 5ns timing accuracy.
- With the FT9-TFC's 50mHz loop bandwidth setting, it merely "follows" the raw 1PPS performance from the receiver. If using a timing receiver that reports quantization error messages, via an external microcontroller, these messages can be used to compensate the error by adjusting the phase in the PLL to offset the predicted location of the next pulse.
- At very long averaging times (e.g., 100,000 seconds), Modified Allan Deviation (MDEV) for an uncompensated 1PPS may appear similar to that of a compensated 1PPS. However, this does not necessarily mean that they perform equally well in a practical holdover scenario.

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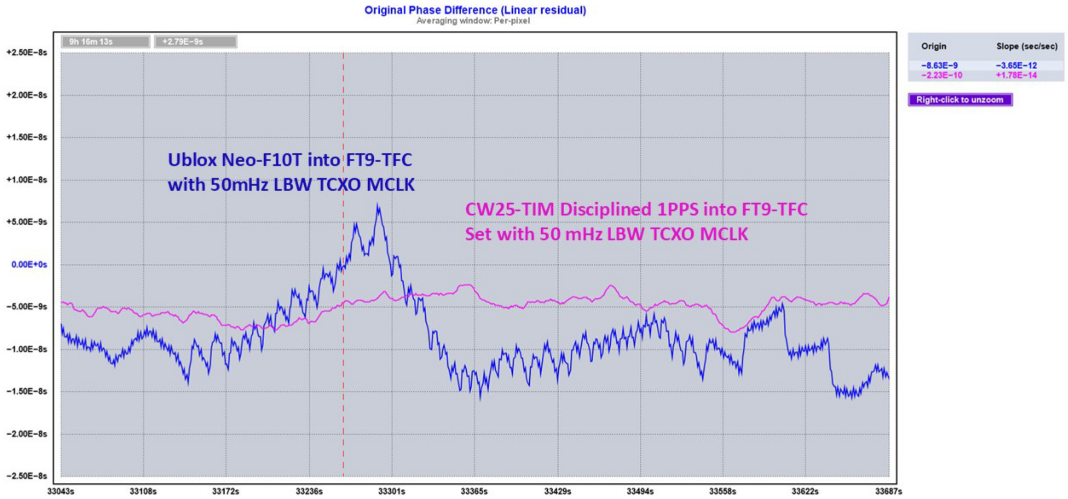
Phase Difference Comparison

Phase Difference and Locking Performance Phase coherence is a critical aspect of timing applications. The FT9 TFC's phase-locked loop (PLL) performance improves with quantization error correction implemented, improving the locking stability when using the same MLCK oscillator.

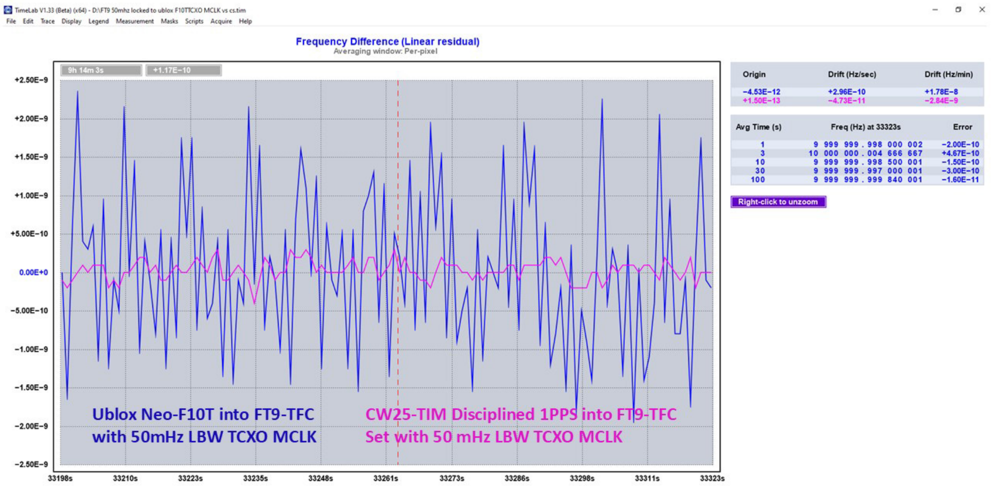
- TCXO MLCK with 50mHz LBW setting supports "lock" condition on the 1PPS of both receiver options, but the phase stability performance looks dramatically different.
- Using the same 50mHz loop bandwidth setting shows markedly improved results when implementing quantization error correction versus the raw 1PPS directly from a "good" timing receiver like the Ublox 10 series specified with a 5ns timing accuracy.



Origin	Slope (sec/sec)
−8.63E−9	−3.65E−12
−2.23E−10	+1.78E−14

Frequency Difference Comparison

- Short-term frequency fluctuations are best observed in the sub-ppb range, as derived from Time Lab calculations but the frequency stability performance between the two looks dramatically different as seen in the Frequency Difference plot below.
- Using the same 50mHz loop bandwidth setting shows markedly improved results when implementing quantization error correction versus the raw 1PPS directly from a "good" timing receiver like the Ublox 10 series specified with a 5ns timing accuracy.



Origin	Drift (Hz/sec)	Drift (Hz/min)
−4.53E−12	+2.96E−10	+1.78E−8
+1.50E−13	−4.73E−11	−2.84E−9

Avg Time (s)	Freq (Hz) at 33323s	Error
1	9 999 999 . 998 000 002	−2.00E−10
3	10 000 000 . 004 666 667	+4.67E−10
10	9 999 999 . 998 500 001	−1.50E−10
30	9 999 999 . 997 000 001	−3.00E−10
100	9 999 999 . 999 840 001	−1.60E−11

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Quantization Error Correction and its impact on Holdover Events

Quantization error correction plays a critical role in maintaining accurate time during holdover events in timing systems. Without compensation, phase and frequency deviations accumulate due to digital resolution limits, leading to increased instability.

While MDEV at 100,000s might suggest similar long-term stability between compensated and uncompensated 1PPS, only the compensated system ensures minimal initial phase and frequency bias, which is critical for meeting strict time accumulation limits in holdover.

When a timing system locks to a 1PPS (one pulse per second) source that is not compensated for sawtooth error, it introduces additional phase noise and frequency instability, which significantly impacts holdover performance. This is particularly concerning when trying to maintain a strict time accumulation limit, such as 1.5 microseconds over 24 hours.

Example: Accumulated Time Error Over 24 Hours

- Suppose an uncompensated 1PPS leads to a slight frequency offset of 1 ppb (10) due to residual sawtooth effects.
- Over 24 hours (86,400 seconds), this results in a drift of: t=frequency offset×time\Delta t = \text{frequency offset} \times\text{time}t=frequency offset×time =(1×10−9)×(86,400 sec)=(1 \times 10^{-9}) \times (86,400 \text{ sec})=(1×10−9)×(86,400 sec) =86.4 microseconds= 86.4 \text{ microseconds}=86.4 microseconds
- If the goal is to keep time error below 1.5 microseconds, even a small initial frequency error can quickly exceed this limit.

This instability results in faster time drift, making it harder to maintain accurate synchronization when GPS is lost. While the underlying stability of the local oscillator (e.g., OCXO, rubidium) ultimately determines long-term drift, effective quantization error correction improves short- and mid-term stability, reducing phase noise and frequency variations. This leads to smoother holdover performance, minimizing time deviation and enhancing overall system reliability.

Conclusion

The FT9 TFC's configurable loop bandwidth and support for various MCLK sources allow users to optimize performance based on their timing requirements. By leveraging advanced sawtooth error correction and low-bandwidth filtering, the FT9-TFC ensures superior phase stability and frequency accuracy, making it an excellent choice for precision timing applications.

The included performance plots illustrate these benefits, providing a clear roadmap for selecting the best FT9 TFC configuration for your needs.

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